IS-550R2UPD8UC
Redundant Power Supply

(CRPS 2U 550W 1+1)

SPECIFICATION

Revision: 0.1

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Revision History

Version	Date	Revision Description	
0.1	**2019/12/24**	**First Version**	

1. General

This specification defines the performance characteristics and functions of a 550 watts CRPS form factor of switch mode redundant power supply with Active PFC (Power Factor Correction) and PMBus (Power Management Bus). **Support 1+1 operation.**

- 80 PLUS Platinum efficiency
- Active Power Factor PF≧0.95
- 0~50℃ Working Temperature
- Surge: 2KV(L/N-PE) &1KV(L-N)
- Altitude : 5000M
- 1+1 Redundant Design
- PMBus™ communication
- Protections: UVP、OVP、OCP、OTP、SCP
- MTBF > 250,000 hours at 25℃ typical load
- Application: Server, Storage , Networking , IPC
- Meet IEC-62368-1

Electrical Specification

MODEL			IS-550R2UPD8UC
AIRFLOW			Back To Front
INPUT	Voltage Range		90~264Vac
	Operation Voltage		100~240Vac
	Frequency Range		47~63Hz
	AC Current (Full Load)		6A/115Vac,3A/230Vac at full load
	Inrush Current		30A peak @115Vac, 50A peak @230Vac Cold start at full load
	Power Factor(Typ.)		≥0.95/115Vac, ≥0.95/230Vac at full load
	Leakage Current		<3.5mA/240Vac
	Efficiency (Typ.)	20% Load	-
		50% Load	-
		100% Load	85%
		Certification	-

OUTPUT	DC Voltage	+12V	+5V	+3.3V	-12V	+5VSB
	Maximum Load	46A	20A	20A	0.5A	3A
	Minimum Load	1A	0A	0A	0A	0A
	Power Output	550W				
	Ripple & Noise	120mV	50mV	50mV	120mV	50mV
	Output Voltage Tolerance	±5%	±5%	±5%	±5%	±5%
	Line Regulation	±1%				
	Load Regulation	±5%				
	Turn On Time And Rise Time	<3s,20ms@115Vac/230Vac at full load				
	Hold Up Time	≥12ms@115Vac at 70% load				
PROTECTION	Short Circuit Protection	Latch Off				
	Over Current Protection	Latch Off				
	Over Voltage Protection	Latch Off				
ENVIRONMENT	Operation Temperature	0 ~ 50℃				
	Storage Temperature	-40 ~ 80℃				
	Humidity	Operating: 20% ~ 90%RH non-condensing				
		Non-Operating: 5% ~ 95%RH non-condensing				
	TEMP. Coefficient	±0.03%/℃ (0~50℃)				
EMC	FCC CFR Title 47 Part 15 Sub Part B EN55024/EN55032	Conducted Class B Radiated Class B				
HI-POT	Dielectric Withstand Voltage	3sec / 1.5KVAC or 2545VDC with a trigger limit of 10mA.				
SURGE VOLTAGE	EN61000-4-5	Line to Line : 1KV Line-to-Ground: 2KV, Performance Criteria B				
OTHERS	MTBF	250Khrs min SR332(25℃)				
	Dimension	230mm (L) x 76mm (W) x 84mm (H)				
	Weight	1800g				
	AC connector	IEC320 C14 type 3pin connector				
	DC output connector	ATX				

2. AC Input Requirement

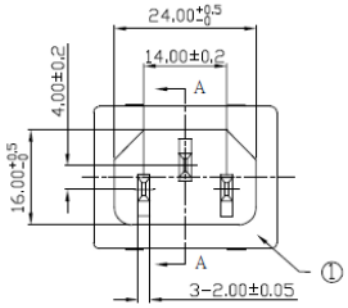
2.1 Input Voltage and Frequency

Voltage (sinusoidal): 100~240 Vac full range, with ±10% tolerance. Input frequency ranges from 47Hz~63Hz

2.2 Input AC Connector

The AC inlet is a IEC320 C14 type 3pin connector. This inlet shall be rated for operation at 10A/250Vac

Figure 1: AC Inlet



2.3 AC Input Current And Inrush Current

AC line inrush current shall not damage any component nor cause the AC line fuse to blow under any DC conditions and with any specified AC line input voltage and frequency. Inrush current is tested at 25 ℃ ambient and cold start within 1/4 AC cycle. Repetitive On/Off cycling of the AC input voltage shall not damage the power supply.

Table 1: Rated output power for each input voltage range

Parameter	Minimum Input	Input Voltage	Maximum Input	Brown In	Brown Out
115Vac	90Vac	100~120Vac	132Vac	85Vac ±5Vac	80Vac ±5Vac
230Vac	180Vac	200~240Vac	264Vac		
Frequency	47Hz	50/60Hz	63Hz		

Table 2: Maximum input current

Input Voltage	Input Current	Maximum Inrush Current	Max Power	Peak Power
90~132Vac	6A@115Vac	30A*peak@115Vac	550W	660W, ≤12ms
180~264Vac	3A@230Vac	50A*peak @230Vac	550W	660W, ≤12ms

*:Redundant Power Module

2.4 Input Power Factor Correction (Active PFC)

The power factor at 100% of rated load shall be ≥ 0.95 at nominal input voltage and full load.

2.5 AC Line Transient Specification

AC line transient conditions are characterized as “sag” and “surge” conditions. Sag conditions (also referred to as “brownout” conditions) will be defined as the AC line voltage dropping below nominal voltage. Surge conditions will be defined as the AC line voltage rising above nominal voltage. The power supply shall meet the regulation requirements under the following AC line sag and surge conditions.

Table 3: AC Line Sag Transient Performance

Duration	Sag	Operating AC Voltage	Line Frequency	Load	Performance Criteria
Continuous	10%	115/230Vac	60/50 Hz	100%	No loss of function or performance
0 - ½ AC cycle	95%	115/230Vac	60/50 Hz	70%	No loss of function or performance
> 1 AC cycle	> 30%	115/230Vac	60/50 Hz	100%	Loss of function Acceptable, Self- recoverable

Table 4: AC Line Surge Transient Performance

Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	115/230Vac	60/50 Hz	No loss of function or performance
0 - ½ AC cycle	30%	115/230Vac	60/50 Hz	

3. DC Output Specification

3.1 Output Power / Current

Table 5: Load Range

Voltage	Condition		
	Min Load	Max Load	
+12V	1A	46A	
+5V	0A	20A	The +3.3, +5 Volt total outputs shall not exceed 150W.
+3.3V	0A	20A	
+5Vsb	0A	3A	
-12V	0A	0.5A	

* The +12V,+3.3V, +5V and -12Volt total outputs shall not exceed 550W.

3.2 Voltage Regulation, Ripple and Noise

Table 6: Regulation, Ripple and Noise

Output Voltage	+12V	+5V	+3.3V	+5Vsb	-12V
Load Reg.	±5%	±5%	±5%	±5%	±5%
Line Reg.	±1%	±1%	±1%	±1%	±1%
Ripple & Noise	120mV	50mV	50mV	50mV	120mV

Ripple and noise shall be measured using the following methods:

- Measurements made differentially to eliminate common-mode noise
- Ground lead length of oscilloscope probe shall be ≤ 0.25 inch.
- Measurements made where the cable connectors attach to the load.
- Outputs bypassed at the point of measurement with a parallel combination of 10uF tantalum capacitor in parallel with 0.1uF ceramic capacitors at each point of measurement. The measurement points shall be as close as possible to the point of load..
- Oscilloscope bandwidth of 0 Hz to 20MHz.
- Measurements measured at locations where remote sense wires are connected.
- Regulation tolerance shall include temperature change, warm up drift and dynamic load

3.3 Capacitive Loading

The power supply shall operate within specifications over the capacitive loading ranges defined below in

Table 7: Capacitive Loading Conditions

Output	MIN	MAX	Units
+12V	10	11,000	uF
+5V	10	12,000	uF
+3.3V	10	12,000	uF
+5Vsb	1	350	uF
-12V	1	350	uF

3.4 Dynamic Loading

The output voltages shall remain within the limits specified in Table-Regulation, ripple and noise for the step loading and within the limits specified in Table-Transient Load Requirement for the capacitive loading. The load transient repetition rate shall be tested between 50Hz and 5kHz at duty cycle 50%. The load transient repetition rate is only a test specification. The ∆ step load may occur anywhere within the MIN load to the MAX load shown in Table-Load Range.

Table 8: Transient Load Requirements

Output	∆Step Load Size	Load Slew Rate	Capacitive Load
+12V	50% of Max. Load	0.5 A/uS	2200 uF
+5V	30% of Max. Load	0.5 A/uS	1000 uF
+3.3V	30% of Max. Load	0.5 A/uS	1000 uF
+5Vsb	50% of Max. Load	1.0 A/uS	20 uF

3.5 Overshoot at Turn-on/Turn-off

Any output overshoot at turn on shall be less than 10% of the nominal output value. Any overshoot shall recover to be within regulation requirements in less than 10ms.

3.6 Timing Requirements

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (Tvout_rise) within 1 to 20ms. For 5Vsb, it is allowed to rise from 1 to 25ms.Both outputs must rise monotonically. Refer to Figure 2 below which shows the timing requirements for the power supply being turned on and off via the input power, with PSON held low and the PSON signal, with the input power applied.

Figure 2: Turn On/Off Timing

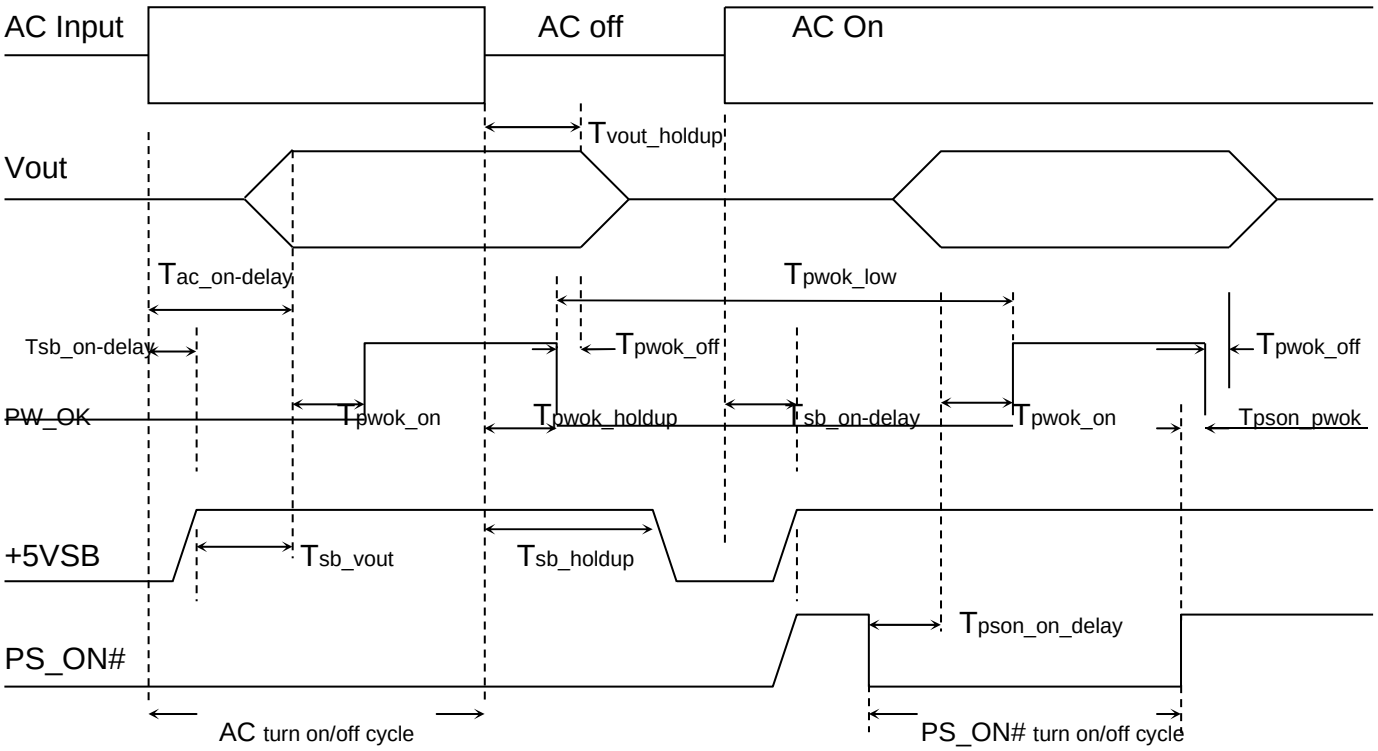


Table 9: Timing Requirements

Item	Description	MIN	MAX	UNITS
Tvout_rise	Output voltage rise time from each main output	1	20	mS
	Output voltage rise time for the +5Vsb output	1	25	mS
Tsb_on-delay	Delay from AC being applied to +5Vsb being within regulation.		1500	mS
Tac_on-delay	Delay from AC being applied to all output voltages being within regulation.		2500	mS
Tvout_holdup	Time all output voltage stay within regulation after loss of AC tested at 70% load.	12		mS
Tpwok_holdup	Delay from loss of AC deassertion of PW_OK tested at 70% load.	11		mS
Tpson_on_delay	Delay from PS_ON# active to output voltage within regulation limits.	5	400	mS
Tpson_pwok	Delay from PS_ON# deactive to PW_OK being deasserted.		50	mS
Tpwok_on	Delay from output voltage within regulation limits to PW_OK asserted at turn on.	100	500	mS
Tpwok_off	Delay from PW_OK deasserted to output voltages dropping out of regulation limits measured at 70% of maximum load..	1		mS
Tpwok_low	Duration of PW_OK being in the deasserted state during an off/on cycle using AC or the PSON# signal. .	100		mS
Tsb_vout	Delay from +5Vsb being in regulation to O/Ps being in regulation at AC turn on.	50	1000	mS

3.7 Control Signal and Other DC Signals

3.7.1 PG Signal (PW_OK)

The power supply shall provide TTL compatible PW_OK signal to the system. Low pass filter (104 capacitor is recommended) shall be added into the PW_OK signal to suppress the high frequency noise to keep the high level absolutely. However, this low pass filter shall be used in PSU or motherboard PW_OK circuit. Therefore, supplier must be subject to add this low pass filter in the PW_OK input circuit of motherboard if it cannot be added in PSU circuit due to the re-layout difficulty.

Table 10: PW_OK TTL Characteristics

Signal Type	TTL Compatible Output Signal	
PW_OK = High	Power OK	
PW_OK = Low	Power Not OK	
	MIN	MAX
Logical low voltage , Isink = 4mA	0V	0.4V
Logical high voltage , Isource = 4mA	2.4V	3.46V
PW_OK rise and fall time	-	100uS
High-state output impedance	Internal PSU to provide a pull-up resistor between 5Vsb and PW_OK	

3.7.2 PS_ON# Signal

PS_ON# signal is required to remotely turn on/off the power supply module / PDB Combo. PS_ON# is an active low signal that turns on the +12V power rail and other DC to DC converters on the PDB. When this signal is not pulled low by the system, or left open, all the outputs (except for 5Vsb) shall be turned off. This signal is pulled to a 5Vsb voltage by a pull-up resistor internal to the PDB. Refer to Figure 2 On/Off Timing for timing diagram.

Table11: PS_ON# TTL Signal Characteristics

Signal type	Accepts an open collector/drain input from the system. Pull-up to 5Vsb located in power supply.	
PS_ON# = Low	Power ON	
PS_ON# = Open or High	Power OFF	
	MIN	MAX
Logic level low (power supply ON)	0V	0.8V
Logic level high (power supply OFF)	2.4V	3.46V
Source current, Vpson = low	-	4mA

Note: When the ON / OFF switching of the PS_ON# signal, Interval cycle time must be > 1Sec.

3.7.3 SMB_Alert# Signal

This signal indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events and that power supply is operating in an environment exceeding the specified limits. This signal is to be asserted in parallel with LED turning solid red.

Table12: SMB_ALERT# Signal Characteristics

Signal Type (Active Low)	TTL Compatible Output Signal	
SMB_Alert# = High	OK	
SMB_Alert# = Low	Alert to System	
	MIN	**MAX**
Logic level low voltage, Isink=4 mA	0V	0.4V
Logic level high voltage, Isource=50uA	2.0V	3.46V
Sink current, SMB_Alert# = low	-	4mA
Source current, SMB_Alert# = high	-	50uA
SMB_Alert# rise and fall time	-	100uS

3.7.4 SCL and SDA Signal

PMBus device uses System Management Bus (SMBus) Version 2.0, for transport layer, which is a two-wire communication protocol based on I2C. Both SCL and SDL lines are bi-directional, connected to a positive supply voltage through a pull-up resistor or a current source.

Table13: SCL and SDA Signal Characteristics

Signal Type	TTL Compatible	
Operating Frequency	100KHz/400KHz	
	MIN	**MAX**
Data Clock Input Low Voltage, (Vil)	0V	0.8V
Data Clock Input High Voltage (Vih)	2.4V	VDD
Data Clock Output Low Voltage (Vol)	-	0.4V
Input Leakage (Ileak)	-	±5uA
Current Through Pull-Up Resistor Or Current Source (Ipullup)	-	4mA
Nominal Bus Voltage (VDD)	-	3.46V

Note: For proper I2C communication, system designer must take account of all I2C devices connected to I2C bus and calculate appropriate pull-up resistors value that satisfy with above rating.

3.7.5 TTL Indicators

There shall be an open-collect TTL to indicate power supply status. The TTL shall pull high to 3.3V indicate that all the power outputs are available or one module is dummy. The TTL shall pull low(under 0.8V) indicate that one module has failed or shutdown due to protection. The standard backplane provides a single TTL output signal.

Power system condition	TTL Status
No AC input power to one power module	Low
One power module not inserted or pulled out	Low
AC Input present/only standby mode	Low
Power module PS ON and output normal	High
Any power module failure	Low

3.8 Efficiency

The power supply must be not less than 85% efficient at maximum load, tested at 230Vac/50Hz Input at 25 deg ambient condition.

FAN power is not included into total power consumption.

Efficiency as follows :

Table 14: Efficiency

Load	20% @230Vac	50% @230Vac	100% @230Vac
Efficiency (Module)	-	-	85%

4. Protection Circuits

Protection circuits inside the power supply shall cause only the power supply's main outputs to shutdown. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15 sec and a PSON# cycle HIGH for 1 sec must be able to restart the power supply.

4.1 Over Current Protection (OCP)

The power supply shall have current limit to prevent the +12V outputs from exceeding the values shown in ***Table-Over Current Protection.*** The power supply shall latch off if the current exceeds the limit.

Voltage	Minimum	Maximum	Shutdown Mode
5VSB	3.6A	5A	Auto-recovery
+12V , +5V , +3.3V	110%	130%	Latch Off

Table 15: Over Current Protection

4.2 Over Voltage Protection (OVP)

The power supply is protected against over voltage due to an internal regulator failure. When an over voltage condition is detected, all DC outputs are disabled (except the +5Vsb). The fault must be removed to restore the DC outputs. The Limits set forth in the following table.

Table 16: Over Voltage Protection

Voltage	Minimum	Maximum	Shutdown Mode
+12V	+13.3V	+14.5V	Latch Off
+5V	+5.5V	+6V	Latch Off
+3.3V	+3.9V	+4.5V	Latch Off

4.3 Short Circuit Protection

- The power supply shall be no physical damage when +12V, +3.3V and +5V, is shorted to its DC return.
- +5Vsb shall be Auto Restart when short condition is removed.

4.4 No Load Operation

No damage or hazardous condition should occur with all the DC output connectors disconnected from the load.

4.5 Over Temperature Protection (OTP)

The power supply will be Auto Recovery when an over temperature condition is removed; no damage shall be caused.

5. Environmental Requirements

5.1 Temperature

Operating Ambient, normal mode (inlet air): 0°C ~ 50°C (32°F~ 122°F)

Non-operating Ambient:: -40°C ~ 80°C (-40°F~ 176°F)

5.2 Humidity

Operating: 20% ~ 90%RH non-condensing

Non-Operating: 5% ~ 95%RH non-condensing

5.3 Altitude

Operating: 16,404 ft (5000M)

5.4 Mechanical Shock

Non-Operating: 50 G Trapezoidal Wave, 11mS half sin wave. The shock is to be applied in each of the orthogonal axes.

5.5 Vibration (Non-Operating)

The power supply shall be subjected to a vibration test consisting of a 10 to 300 Hz sweep at a constant acceleration of 2.0g for duration of one (1) hour for each of the perpendicular axes X, Y and Z (0.1 octave/minute). The output voltages shall remain within specification.

5.6 Reliability

The MTBF of the power supply shall be calculated utilizing the Part-Stress Analysis method of SR332. The calculated MTBF of the power supply shall be greater than 250,000 hours under the following Conditions: Full rated load; 120Vac input; 25°C; ; Without Fan

5.7 Electromagnetic Compatibility

Table 17: EMC Requirements

Electromagnetic Interference	FCC CFR Title 47 Part 15 Sub Part B EN55032/EN55024	Conducted Class B Radiated Class B		
Harmonics	IEC61000-3-2 Class D			
Flicker	IEC61000-3-3			
ESD Susceptibility	EN-61000-4-2	±8KV by Air, ±4KV by Contact Performance Criteria B		
Radiated Susceptibility	EN61000-4-3	80MHz~1000MHz (3V/m(mns) Amplitude 80% AM 1KHz Criteria A		
EFT/Burst	EN61000-4-4	5KHz, AC: 1KV, DC: 0,5 KV, Performance Criteria B		
Surge Voltage	EN61000-4-5	Line to Line : 1KV Line-to-Ground: 2KV, Performance Criteria B		
Conducted Susceptibility	EN61000-4-6	50 Hz/3A(ms)/m Performance Criteria A		
RF Conducted	EN61000-4-8	0.15MHz~80MHz 3V/m Amplitude 80% AM 1KHz Performance Criteria A		
Voltage Dips and Interruptions	EN61000-4-11	30%(Voltage Dips) 60%(Voltage Dips) >95%(Voltage Dips)	10 ms 100ms 500ms	Criteria B Criteria C Criteria C
Leakage Current	EN60950-1	3.5mA@240Vac		

5.8 Safety Agency Requirements

This power supply is designed to meet the following safety

Table 18: Product Safety

Product Safety:	• CB: IEC 60950-1:2005 (2nd Edition); Am 2:2013 • TUV: EN60950-1/A12:2011 • UL: UL60950-1, 2nd Edition, 2011-12-19 • UL62368-1, 2nd Edition, 2014-12-01 • CCC: GB4943.1-2011 GB9254-2008 GB17625.1-2003 • IEC62368-1

6. PMBus Command Codes

6.1 PMBus Command Codes For Module

(Detailed settings, please refer to the Module Description)

6.2 PMBus Command Codes For PDB

Table 20 – PMBus Command Codes (PDB)

Command Code	Command Name	SMBus Transaction Type	Number of Data Bytes	Decode Format
00h	PAGE	R/W Byte	1	U8
03h	CLEAR_FAULTS	Send Byte	0	-
19h	CAPABILITY	Read Byte	1	Byte
20h	VOUT_MODE	Read Byte	1	Byte
1Ah	QUERY	Process Call	1	Byte
79h	STATUS_WORD	Read Word	2	Word
7Ah	STATUS_VOUT	Read Byte	1	Byte
7Bh	STATUS_IOUT	Read Byte	1	Byte
7Dh	STATUS_TEMPERATURE	Read Byte	1	Byte
8Bh	READ_VOUT	Read Word	2	Linear Vout
8Ch	READ_IOUT	Read Word	2	Linear
8Dh	READ_TEMPERATURE_1	Read Word	2	Linear
96h	READ_POUT	Read Word	2	Linear
99h	MFR_ID	Block Read	8	ASCII
9Ah	MFR_MODEL	Block Read	13	ASCII
9Bh	MFR_REVSION	Block Read	2	ASCII
9Eh	MFR_SERIAL	Block Read	13	ASCII
A7h	MFR_POUT_MAX	Read Word	2	Linear
A8h	MFR_TAMBIENT_MAX	Read Word	2	Linear

➢ PAGE Command (00h)

The page command provides the ability to configure, control and monitor through only one physical address either:

- Multiple outputs on one unit or

-Multiple non-PMBus devices through a PMBus device to non-PMBus device adapter or bridge.

Pages 00h through 1Fh are reserved specifically for multiple outputs on a device with a single physical address.

PMBUS command valid for PAGE member:

READ_VOUT

READ_IOUT

READ_POUT

STATUS_VOUT

STATUS_IOUT

Table 21 : PAGE Command (00h)

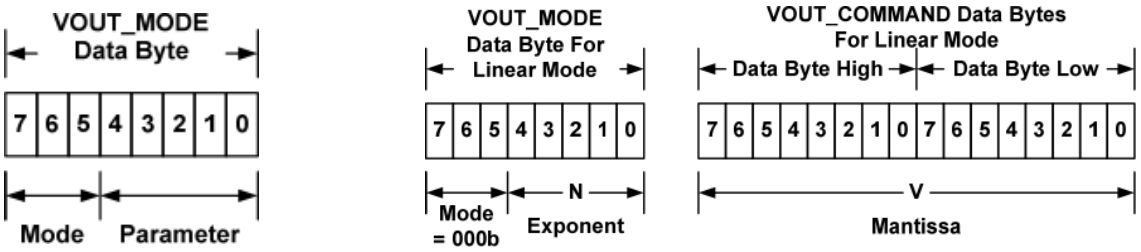
PAGE	READ_VOUT	READ_IOUT	READ_POUT	STATUS_VOUT	STATUS_IOUT
00h	12V	12V	12V	12V	12V
01h	VSB	VSB	VSB	VSB	VSB
02h	5V	5V	5V	5V	5V
03h	3.3V	3.3V	3.3V	3.3V	3.3V
04h	-12V	X	X	-12V	X

Table 22 : Contents in 19h (CAPABILITY)Command Code

Bit Number	Value	Meaning
7	1	Packet Error Checking is supported
[6:5]	00b	Maximum supported bus speed is 100 kHz
4	1	The device does have a SMBALERT# pin and does support the SMBus Alert Response protocol
[3:0]	X	Reserved

Table 23 : Contents in 20h (VOUT_MODE) Command Code

Mode	Bits [7:5]	Bits [4:0] (Parameter)
Linear	000b	Five bit two's complement exponent for the mantissa delivered as the data bytes for an output voltage related command.



Note:

The Mode bits are set to 000b.

The Voltage(ex.12V_OUT , VSB_OUT), in volts, is calculated from the equation:

Voltage = V x 2^n

Where:

Voltage is the parameter of interest in volts;

V is a 16 bit unsigned binary integer; and

N is a 5 bit two's complement binary integer.

Table 24: Contents in 1Ah (QUERY)Command Code

Bit Number	Value	Meaning
7	1	Command is supported
6	1	Command is supported for write
5	1	Command is supported for read
[4:2]	000b	Linear Data Format used
[1:0]	X	Reserved

Table 25: Contents in 79h (STATUS_WORD)Command Code

Byte	Bit Number	Status Bit Name	Meaning
Low	7	Reserved	Return=0
	6	OFF	The Unit Main Power OFF = 1 ;Power ON = 0;
	5	VOUT_OV_FAULT	An output overvoltage fault has occurred = 1 ; Normal = 0
	4	IOUT_OC_FAULT	An output overcurrent fault has occurred = 1; Normal=0
	3	Reserved	Return=0
	2	Temperature	A Temperature fault or warning has occurred=1; Normal=0
	[1:0]	Reserved	Return=0
High	7	VOUT	An output voltage fault or warning has occurred=1; Normal=0
	6	IOUT	An output current fault or warning has occurred=1; Normal=0
	5	Reserved	Return=0
	4	Reserved	Return=0
	3	POWER_ GOOD#	The POWER_GOOD signal is OK = 0;FAIL = 1
	2	Reserved	Return=0
	[1:0]	Reserved	Return=0

Table 26 : Contents in 7Ah (STATUS_VOUT)Command Code

Bit Number	Status Bit Name	Meaning
7	VOUT_OV_FAULT	Normal = 0 12V_V > 13.4V 5V_V > 5.75V 3.3V_V > 3.8V N12V_V > -10.8V = 1 ;
6	VOUT_OV_WARNING	Normal = 0 12V_V > 12.6V 5V_V > 5.5V 3.3V_V > 3.63V N12V_V > -11.4V = 1 ;
5	VOUT_UV_WARNING	Normal = 0 12V_V < 11.4V 5V_V < 4.5V 3.3V_V < 2.97V N12V_V < -12.6V = 1 ;
4	VOUT_UV_FAULT	Normal = 0 12V_V < 10.8V 5V_V < 3.75V 3.3V_V < 2.5V N12V_V < -13.4V = 1 ;
[3:0]	Reserved	Return=0

Table 27: Contents in 7Bh (STATUS_IOUT)Command Code

Bit Number	Status Bit Name	Meaning
7	IOUT_OC_FAULT	Normal = 0 12V_I > 56A 5V_I > 26A 3.3V_I > 26A = 1 ;
6	Reserved	Return=0
5	IOUT_OC_WARNING	Normal = 0 12V_I > 56A 5V_I > 22A 3.3V_I > 22A = 1 ;
[4:1]	Reserved	Return=0

Table 28: PDB PMBUS Adrress

PDB address	
IPMI FRU Device(Optional)	**0xAC**
MCU Device	**0xBE**

Note : PMBus device of addressing the above specifications are 8-bit Description

6.2.3 Sensor Accuracy

The sensor of the power supply shall meet below accuracy requirements for sensor readings.

Full-scale Accuracy			Full-scale Value
Item	Load ≤ 20%	Load > 20%	
Vin	±5%	±5%	264Vac
Iin	±10%	±5%	6.5A
Pin	±10%	±5%	650W
Vout	±5%	±5%	12.6V
Iout	±5%	±5%	46A
Pout	±5%	±5%	550W
Temp.	±5℃	±5℃	N/A

Note : Full-scale Accuracy (%FS)= (Difference Value / Full-scale Value) x 100%

Appendix I. Data Format Description

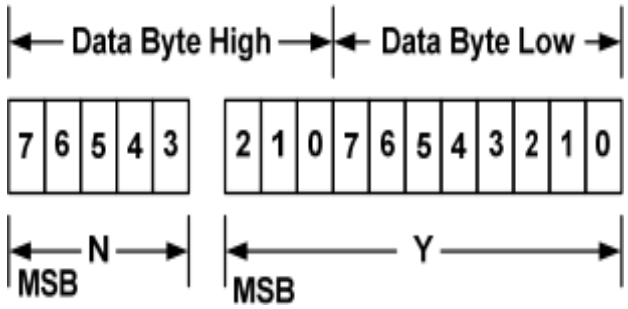
The Linear Data Format is typically used for commanding and reporting the parameters such as (but not only) the following:

- Input Voltage (V)
- Input Current (A)
- Input Power (W)
- Output Current (A)
- Output Power(W)
- FAN Speed (RPM)
- Temperature(℃)
- Any Warning Limit

The Linear Data Format is a two byte value with:

An 11 bit, two's complement mantissa and a 5 bit, two's complement exponent (scaling factor).

The format of the two data bytes is illustrated in Figure



The relation between Y, N and the "real world" value is:

$X = Y \cdot 2^N$

Where, as described above:

X is the "real world" value;

Y is an 11 bit, two's complement integer; and

N is a 5 bit, two's complement integer.

Devices that use the Linear format must accept and be able to process any value of N.

7. MFR Information

Table 29 MFR Meaning

(Detailed settings, please refer to the Module Description)

Table 30 MFR Meaning (For PDB)

Command Code	Command Name	Meaning
99h	MFR_ID	Xeal
9Ah	MFR_MODEL	IS-550R2UPD8UC
9Bh	MFR_REVSION	A0 ~ Z9
9Eh	MFR_SERIAL	TYMMEXXXX1234 (Digit = 13)
A7h	MFR_POUT_MAX	550 (W)
A8h	MFR_TAMBIENT_MAX	50 (°C)

8. FRU Data Format (Optional)

For identification of the power supply an internal 256x8 bit EEPROM with PMBus interface is used.The information in the EEPROM follows the IPMI (Platform Management FRU Information Storage Definition) guidelines Document Revision 1.1 from November 15, 1999 and Siemens Norm SN77250. The PSU's FRU Data is specified as the contents attached in the end.

9. LED Indicators

There will be a LED on each power module to indicate power status

(Detailed settings, please refer to the Module Description)

10. Buzzer Indicators

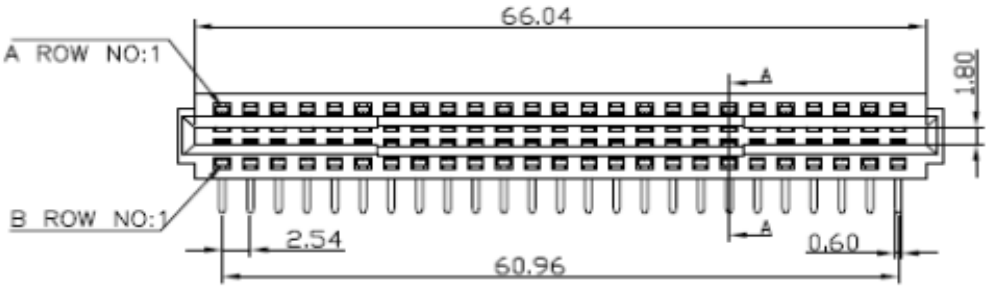
The backplane has an audio buzzer to indicate that one module has failed or shutdown due to protection. The warning buzzer will sound continuously. It can reset warning buzzer by pressing the buzzer reset switch or by shorted (pull low) the buzzer reset connector.

Power system condition	Backplane Buzzer Status
No AC input power to one power module only after PS ON	Steady buzzing
One power module not inserted or pulled out	Steady buzzing
AC Input present/only standby mode	OFF
Power module PS ON and output normal	OFF
Any power module failure after PS ON	Steady buzzing

11.PDB Mating Connector

The power supply shall have a card edge to mate with the Low Profile Hybrid Power connector Interconnect system. The Matting connector at PDB side is Oupiin 9393-F4P50N11ACB30DA

Figure 3: DC Connector



11.1 Pin Assignment of DC Connector

Figure 4 – Card Edge Pin Out Location

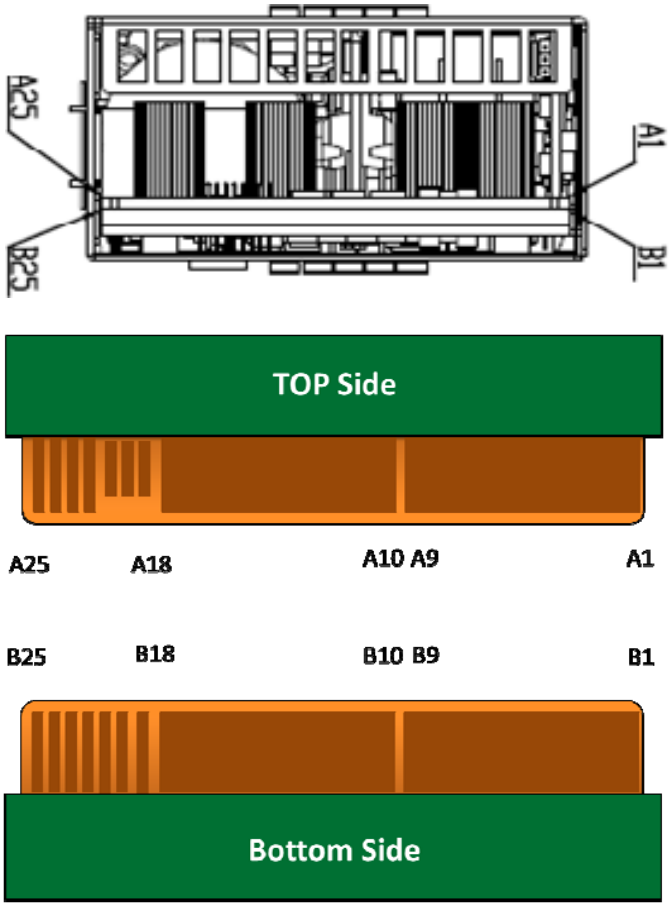


Table 31– Card Edge Pin Out Definition

Bottom Side			
Pin Name	**Signal Name**	**Function**	**System/Backplane Connection**
B1	GND	Grounding	System GND
B2	GND	Grounding	System GND
B3	GND	Grounding	System GND
B4	GND	Grounding	System GND
B5	GND	Grounding	System GND
B6	GND	Grounding	System GND
B7	GND	Grounding	System GND
B8	GND	Grounding	System GND
B9	GND	Grounding	System GND
B10	+12V	+12V power output	To System 12V BUS
B11	+12V	+12V power output	To System 12V BUS
B12	+12V	+12V power output	To System 12V BUS
B13	+12V	+12V power output	To System 12V BUS
B14	+12V	+12V power output	To System 12V BUS
B15	+12V	+12V power output	To System 12V BUS
B16	+12V	+12V power output	To System 12V BUS
B17	+12V	+12V power output	To System 12V BUS
B18	+12V	+12V power output	To System 12V BUS
B19	A0(SMBus address)	See Table 35	From the system settings
B20	A1(SMBus address)		
B21	12VSB	+12VSB Power output	To System 12VSB BUS
B22	Cold Redundancy Bus	See application note for detail	Connect pin to pin at backplane for each power module
B23	12LS	12V Load Share	Connect pin to pin at backplane for each power module. See table 40 for details
B24	PRESENT	Indicate if a power has been plugged in.	Floating via backplane.
B25	Compatibility Check pin	The power supply shall use one pin on the output connector to check that a power supply is compatible before powering on in the system. This is accomplished via a bus connected between all power supplies in the system. One power supply in the system shall provide a voltage on the compatibility bus; the others shall see if the voltage is the same as what it expects for compatibility before powering ON their main outputs. See table 41 for voltage range.	

Table 32 Card Edge Pin Out Definition

TOP Side			
Pin Name	**Signal Name**	**Function**	**System/Backplane Connection**
A1	GND	Grounding	System GND
A2	GND	Grounding	System GND
A3	GND	Grounding	System GND
A4	GND	Grounding	System GND
A5	GND	Grounding	System GND
A6	GND	Grounding	System GND
A7	GND	Grounding	System GND
A8	GND	Grounding	System GND
A9	GND	Grounding	System GND
A10	+12V	+12V power output	To System 12V BUS
A11	+12V	+12V power output	To System 12V BUS
A12	+12V	+12V power output	To System 12V BUS
A13	+12V	+12V power output	To System 12V BUS
A14	+12V	+12V power output	To System 12V BUS
A15	+12V	+12V power output	To System 12V BUS
A16	+12V	+12V power output	To System 12V BUS
A17	+12V	+12V power output	To System 12V BUS
A18	+12V	+12V power output	To System 12V BUS
A19	SDA	I2C DATA	To Syetem I2C BUS
A20	SCL	I2C CLOCK	To Syetem I2C BUS
A21	PSON	Module PSON. Remote control power On/Off (Pulled LOW = POWER ON)	From System On/Off Controller
A22	SMB_ALERT	If PSU FAIL,FAN FAIL,OCP occurs, signal will be pulled from High to Low , PSU normal =High(TTL LEVEL)	To system related bus
A23	RETURN_S	+12V Remote sense For GND	To System GND
A24	+12VRS	+12V Remote sense	To System 12V BUS
A25	PWOK	Power Good Output. Signal is pulled HIGH by PSU to indicate all outputs ok.	To System Power Good

Table 33:Load Share Voltage Range (B23 PIN)

Parameter Description (For single output of +12V)	Min	Typ	Max
Vishare Voltage, 50% load	3.8V	4V	4.2V
Vishare Volatge, 100% laod	7.7V	8V	8.3V

Table 34:Compatibility Voltage Range (B25 PIN)

Description	Min	Typ	Max
Compatibility Check pin	1.65V	1.8V	1.95V

Figure 5 Power Supply Compatibility Bus Voltage Chart

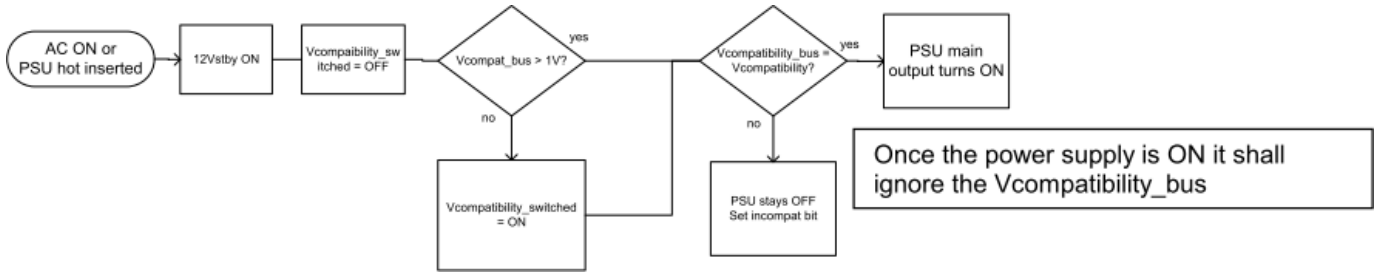


Table 35 I²C Address Set Table(For Module)

PSU address A1/A0	0/0 (PSU1)	0/1 (PSU2)
IPMI FRU Device (Optional)	**A0**	**A2**
MCU Device	**B0**	**B2**

Table 36: I²C Address Set Table(For PDB)

PDB address	
IPMI FRU Device(Optional)	**0xAC**
MCU Device	**0xBE**

Note : PMBus device of addressing the above specifications are 8-bit Description

12. Mechanical Drawing

Size: 230mm (L) x 76mm (W) x 84mm (H)