

IX-400RSH1UP8UC

IX-400RSH1UP8UC

Active PFC/Full Range Input

(1U 400W 1+1 Redundant)

SPECIFICATION

Revision: 1.0

3500 E. Francis St. Ontario, CA 91761. USA http:// www.Xeal.com.tw

TEL: 626-303-8885 FAX: 626-301-0588

1 GENERAL SCOPE

This specification defines the performance characteristics of a grounded, AC input, 400 watts, 5 output level power supply. This specification also defines worldwide safety requirements and manufactures process test requirements.

2 Power Input Specification

2.1 Input Voltage

The power supply must operate within all specified limits over the following input voltage range. The power supply shall operate properly at 85 VAC input voltage to guarantee proper design margins.

| PARAMETER | MIN | RATED | MAX | PEAK |
|---------------|----------|----------------|----------|------|
| Voltage (110) | 90 Vrms | 100 – 127 Vrms | 140 Vrms | |
| Current | | 6A N | 1ax. | |
| Voltage (220) | 180 Vrms | 200 – 240 Vrms | 264 Vrms | |
| Current | | 3A Max. | | |
| Frequency | 47 Hz | 50 – 60 Hz | 63 Hz | |

2.2 AC Inrush Current

AC line inrush current shall not exceed 30A peak(for each power unit), for up to one-quarter of the AC cycle, after which, the input current should be no more than the specified maximum input current. The peak inrush current shall be less than the ratings of its critical components (including input fuse, bulk rectifiers, and surge limiting device).

The power supply must meet the inrush requirements for any rated AC voltage, during turn on at any phase of AC voltage, during a single cycle AC dropout condition as well as upon recovery after AC dropout of any duration, and over the specified temperature range (Top).

2.3 AC Line Dropout / Holdup

An AC line dropout is defined to be when the AC input drops to 0VAC at any phase of the AC line for any length of time. During an AC dropout the power supply must meet dynamic voltage regulation requirements. An AC line dropout of any duration shall not cause tripping of control signals or protection circuits. If the AC dropout lasts longer than the holdup time the power supply should recover and meet all turn on requirements. The power supply shall meet the AC dropout requirement over rated AC voltages and frequencies. A dropout of the AC line for any duration shall not cause damage to the power supply.

| Loading | Holdup Time |
|---------|-------------|
| 100% | 12ms |

2.4 Susceptibility Requirements

The power supply shall meet the following electrical immunity requirements when connected to a cage with an external EMI filter, which meets the criteria defined in the SSI document EPS Power Supply Specification.

| Level | Description | | | |
|-------|---|--|--|--|
| А | The apparatus shall continue to operate as intended. No degradation of performance. | | | |
| В | The apparatus shall continue to operate as intended. No degradation of performance beyond | | | |
| | spec. limits. | | | |
| C | Temporary loss of function is allowed provided the function is self-recoverable or can be | | | |
| | restored by the operation of the controls. | | | |

2.4.1 Electrical Discharge Susceptibility

The power supply shall comply with the limits defined in EN 55024:2010 using the IEC61000-4-2:2009 test standard and performance criteria B defined in Annex B of CISPR 24.

2.4.2 Fast Transient/Burst

The power supply shall comply with the limits defined in EN55024:2010 using the IEC61000-4-4:2012 test standard and performance criteria B define in Annex B of CISPR 24.

2.4.3 Radiated Immunity

The power supply shall comply with the limits defined in EN55024:2010 using the IEC61000-4-3:2006+A1:2008+A2:2010 test standard and performance criteria A defined in Annex B of CISPR 24.

2.4.4 Surge Immunity

The power supply shall be tested with the system for immunity to AC Ring wave and AC Unidirectional wave, both up to 2kV(Differential mode 2K,Common mode 1K), per EN55024:2010,

EN 61000-4-5:2014 and ANSI C63.4:2014.

The pass criteria include: No unsafe operation is allowed under any condition; all power supply output voltage levels to stay within proper spec levels; No change in operating state or loss of data during and after the test profile; No component damage under any condition.

The power supply shall comply with the limits defined in EN55024:2010 using the IEC61000-4-5:2014 test standard and performance criteria B defined in Annex B of CISPR 24.

2.4.5 AC Line Transient Specification

AC line transient conditions shall be defined as "sag" and "surge" conditions. "Sag" conditions are also commonly referred to as "brownout", these conditions will be defined as the AC line voltage dropping below nominal voltage conditions. "Surge" will be defined to refer to conditions when the AC line voltage rises above nominal voltage.

The power supply shall meet the requirements under the following AC line sag and surge conditions.

| Duration | Sag | Operating AC Voltage | Line Frequency | Performance Criteria |
|-------------------|------|---------------------------|----------------|---|
| 0 to 1/2 AC cycle | 95% | Nominal AC Voltage ranges | 50/60Hz | No loss of function or performance |
| >1 AC cycle | >30% | Nominal AC Voltage ranges | 50/60Hz | Loss of function acceptable, self recoverable |

AC Line Sag Transient Performance (10sec interval between each sagging):

AC Line Surge Transient Performance

| Duration | Surge | Operating AC Voltage | Line | Performance Criteria |
|-------------------|-------|----------------------------------|---------|------------------------------------|
| Continuous | 10% | Nominal AC Voltage ranges | 50/60Hz | No loss of function or performance |
| 0 to 1/2 AC cycle | 30% | Mid-point of nominal AC Voltages | 50/60Hz | No loss of function or performance |

2.4.6 AC Line Fast Transient (EFT) Specification

The power supply shall meet the EN61000-4-5 directive and any additional requirements in IEC1000-4-5:1995 and the level 3 requirements for surge-withstand capability, with the following conditions and exceptions:

• These input transients must not cause any out-of-regulation conditions, such as overshoot and undershoot, nor must it cause any nuisance trips of any of the power supply protection

circuits.

- The surge-withstand test must not produce damage to the power supply.
- The supply must meet surge-withstand test conditions underDC- maximum and minimum output load conditions.
- 2.4.7 Power Recovery

The power supply shall recover automatically (auto recover) after an AC power failure. AC power failure is defined to be any loss of AC power that exceeds the dropout criteria.

2.4.8 Voltage Brownout

Input voltage range for AC minimum startup voltage, 81 to 89VAC, and maximum turn off voltage range 71 to 79VAC

2.4.9 AC Line Leakage Current

The maximum leakage current to ground of power supply shall be 3.5mA when tested at 264Vac/60Hz.

2.5 Power factor correction

The power supply modules shall incorporate universal power input with active power factor correction, which shall reduce the line harmonics in accordance with the EN61000-3-2 CLASS "D" standards. Power Factor: Typ. > 95% @115/230Vac, full load.

3 Power Output Specification

3.1 Grounding

The output ground of the pins of the power supply provides the output power return path. The ground output at the PCB card edge shall be connected to the safety ground (power supply enclosure). This grounding should be well designed to ensure passing the max allowed Common Mode Noise levels.

The power supply shall be provided with a reliable protective earth ground. All secondary circuits shall be connected to protective earth ground. This path may be used to carry DC-current.

3.2 Output Rating

| GROUP | 1 | 2 | 3 | 4 | 5 |
|----------------|-------|-----|-------|------|-------|
| OUTPUT VOLTAGE | +3.3V | +5V | +12V | -12V | +5VSB |
| RATED LOAD | 20A | 25A | 32.3A | 0.3A | 2.5A |

| MAX. LOAD | 20A | 25A | 33A | 0.3A | 3.5A |
|-----------------------|-------|-------|------|------|------|
| PEAK LOAD | 20A | 25A | 39A | 0.3A | 4.0A |
| MIN. LOAD | 0A | 0A | 0A | 0A | 0A |
| REGULATION | ±5% | ±5% | ±5% | ±5% | ±5% |
| RIPPLE & NOISE (mV) | 50 | 50 | 120 | 120 | 50 |
| Capacitive Loads (uF) | 12000 | 12000 | 4700 | 350 | 350 |

NOTE:

- The continuous maximum total output power shall not exceed 400W.
- Peak power and current loading should be supported for a minimum of 100ms.
- Combined +3.3V and +5V power shall not exceed 150W.
- The power supply shall meet the voltage regulation under all operating conditions (AC line, transient loading, output loading). These limits include the peak-peak ripple/noise.
- Ripple and Noise measuring with an oscilloscope with 20 MHz bandwidth. Output should be bypassed at the connector with a 0.1uF ceramic disk capacitor and a 10uF electrolytic capacitor to simulate system load. The length of ground wire on probe should not longer than 40mm, if a Non - differential type of scope was used.

3.3 No Load Operation

The power supply shall meet all requirements except for the transient loading requirements when operated at no load on all outputs.

3.4 Dynamic Loading

The output voltages will remain within limits specified in 3.2 Output Voltage Regulation for the step loading and capacitive loading specified in the table below. The load transient repetition rate shall be tested between 50Hz and 5kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load to the MAX load conditions.

| Output | ∆ Step Load Size | Load Slew Rate | Test capacitive Load |
|--------|------------------|----------------|----------------------|
| +3.3V | 30% of max load | 0.5A/µs | 1000uF |
| +5V | 30% of max load | 0.5 A/μs | 1000uF |
| +12V | 65% of max load | 0.5 A/μs | 2200uF |

| +5VSB 25% of max load 0.5 A/μs | 1uF |
|--------------------------------|-----|
|--------------------------------|-----|

3.5 Maximum Load Change

The power supply shall continue to operate normally when there is a step change $\leq 1A/\mu$ sec, between minimum load and maximum load.

3.6 Close loop Stability

The power supply shall be unconditionally stable under all line/load/transient load conditions including capacitive load ranges. A minimum of: 45 degrees phase margin and -10dB gain margin is required.

Closed-loop stability must be ensured at the maximum and minimum loads as applicable.

3.7 Residual Voltage Immunity in Standby mode

The power supply should be immune to any residual voltage placed on its outputs (Typically a leakage voltage through the system from standby output) up to 500mV. There shall be no additional heat generated, nor stressing of any internal components with this voltage applied to any individual or all outputs simultaneously. It also should not trip the protection circuits during turn on.

The residual voltage at the power supply outputs for no load condition shall not exceed 100mV when AC voltage is applied and the PSON# signal is de-asserted.

3.8 Soft Starting

The Power Supply shall contain control circuit which provides monotonic soft start for its outputs without overstress of the AC line or any power supply components at any specified AC line or load conditions.

3.9 Forced Load Sharing

The +12V output will have active load sharing. The output will share within 10% at full load. The failure of a power supply should not affect the load sharing or output voltages of the other supplies still operating. The supplies must be able to load share in parallel and operate in a hot-swap / redundant 1+1 configurations.

| Ishare Voltage | |
|----------------------------|-------------------------|
| % of max. current capacity | Voltage level (+/- 10%) |
| 50% | 4V |

| 100% 8V | |
|---------|--|
|---------|--|

3.10 Overshoot at Turn-on/Turn-off

Any output overshoot at turn on shall be less than 10% of the nominal output value. Any overshoot shall recover to be within regulation requirements in less than 10ms.

3.11 Undershoot at Turn-on/Turn-off

Any output shall not undershoot at turn on or off cycle under any circumstances.

4 Timing

The output voltages rise from 10% to within regulation limits (Tvout_rise) within 5 to 70ms. For 5VSB, it rises from 1 to 25ms. All outputs rise monotonically. Each output voltage shall reach regulation within 50mS (Tvout_on) of each other during turn on of the power supply system. Each output voltage shall fall out of regulation within 400mS (Tvout_off) of each other during turn off.

| ltem | Description | MIN | MAX | Units |
|------------|--|-----|-----|-------|
| Tvout_rise | Output voltage rise time for all main output | | 70 | ms |
| | Output voltage rise time for the 5VSB output | 1 | 25 | ms |
| Tvout_on | All main outputs must be within regulation of each other within this time. | | 50 | ms |
| Tvout_off | All main outputs must leave regulation within this time. | | 400 | ms |

Output Voltage Timing

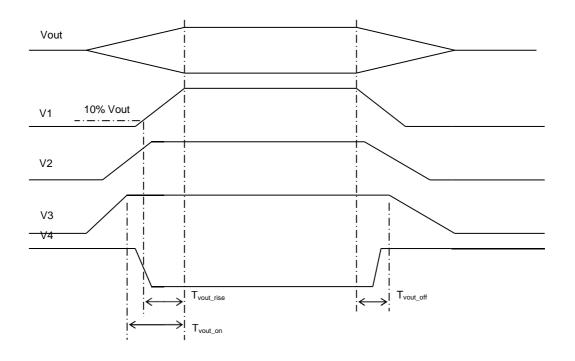
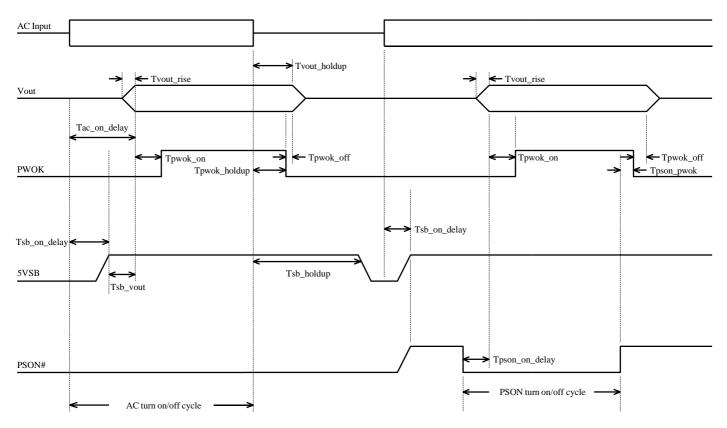


Table below shows the timing for the power supply being turned on and off via the AC input, with PSON held low and the PSON signal, with the AC input applied.

| Item | Description | MIN | MAX | Units |
|----------------|--|-----|------|-------|
| Tsb_on_delay | Delay from AC being applied to 5VSB being within regulation. | | 1500 | ms |
| T ac_on_delay | Delay from AC being applied to all output voltages being within regulation. | | 3000 | ms |
| Tvout_holdup | Time all output voltage stay within regulation after loss of AC. | 13 | | ms |
| Tpwok_holdup | Delay from loss of AC to de-assertion of PWOK. | 12 | | ms |
| Tpson_on_delay | Delay from PSON# active to output voltages within regulation limits. | 5 | 400 | ms |
| T pson_pwok | Delay from PSON# deactivate to PWOK being de-asserted. | | 50 | ms |
| Tpwok_on | Delay from output voltages within regulation limits to PWOK asserted at turn on. | 10 | 500 | ms |

| T pwok_off | Delay from PWOK de-asserted to output | 1 | | ms |
|------------|---|----|------|----|
| | voltages(3.3V, 5V, 12V, -12V) dropping out of | | | |
| | regulation limits. | | | |
| Tpwok_low | Duration of PWOK being in the de-asserted | 10 | | ms |
| | state during an off/on cycle using AC or the | | | |
| | PSON# signal. | | | |
| Tsb_vout | Delay from 5VSB being in regulation to O/Ps | 50 | 1000 | ms |
| | being in regulation at AC turn on. | | | |
| Tsb_holdup | Time 5VSB output voltage stays within | 70 | | ms |
| | regulation after loss of AC | | | |
| Tvout_rise | Output voltage rise time from each main | | 20 | ms |
| | output | | | |

Turn on/off Timing



5 Control And Indicator Functions

5.1 PSON# Input Signal

The PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turns on the main output power rail. When this signal is not pulled low by the system, or left open, the outputs (except the standby output) turn off. This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply.

| Signal Type | Accepts an open collector/drain input from th Pull-up to VSB located in power supply. | |
|-------------------------------------|--|-------|
| PSON# = Low | 0 | N |
| PSON# = High or Open | OI | FF |
| | MIN MAX | |
| Logic level low (power supply ON) | 0V | 1.0V |
| Logic level high (power supply OFF) | 2.0V | 3.46V |
| Source current, Vpson = low | | 4mA |
| Power up delay: Tpson_on_delay | 5ms | 400ms |
| PWOK delay: T pson_pwok | | 50ms |

5.2 PWOK (Power OK) Output Signal

PWOK is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. The start of the PWOK delay time shall inhibited as long as any power supply output is in current limit.

| Signal Type | Open collector/drain ou | Open collector/drain output from power supply. | | |
|--------------------------------------|---------------------------|--|--|--|
| | Pull-up to VSB located in | the power supply. | | |
| PWOK = High | Pov | ver OK | | |
| PWOK = Low | Powe | r Not OK | | |
| | MIN | MAX | | |
| Logic level low voltage, Isink=400uA | 0V | 1.0V | | |
| Logic level high voltage | 2.0V | 3.46V | | |
| Sink current, PWOK = low | | 400μΑ | | |
| Source current, PWOK = high | | 2mA | | |
| PWOK delay: Tpwok_on | 100ms | 500ms | | |
| PWOK rise and fall time | | 100µs | | |
| Power down delay: Tpwok_off | 1ms | | | |

5.3 SMBAlert# SIGNAL (Optional)

This signal indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events. The signal shall activate in the case of critical component temperature reached a warning threshold, general failure, over-current, over-voltage, under-voltage, failed fan. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits.

This signal is to be asserted in parallel with LED turning solid Amber or blink Amber.

| Signal Type (Active Low) | Open collector / drain output from power supply. Pull-up to VSB located in system. | | |
|--------------------------------------|---|-------|--|
| Alert# = High | C | Ж | |
| Alert# = Low | Power Alert to system | | |
| | MIN | MAX | |
| Logic level low voltage, Isink=4mA | 0V | 1.0V | |
| Logic level high voltage, Isink=50µA | 2.0V 3.46V | | |
| Sink current, Alert# = low | | 4mA | |
| Sink current, Alert# = high | | 50µA | |
| Alert# rise and fall time | | 100µs | |

5.3.1 A0

PSU Module Address Line 0. This signal line is provided for determining the address for the specific PSU FRU and SMBus address. The pull-up resister should be located in the system and the pull-up voltage should be limited to 3.3V.

The address line should be pull low with equal to or less than 100 ohm in the motherboard design.

5.3.2 A1

PSU Module Address Line 1. This signal line is provided for determining the address for the specific PSU FRU and SMBus address. The pull-up resister should be located in the system and the pull-up voltage should be limited to 3.3V.

The address line should be pull low with equal to or less than 100 ohm in the motherboard design.

5.4 SCL and SDA

One pin is the serial clock (SCL), and the other pin is used for serial data (SDA). The SCL and SDA

signals are pulled up by system, both pins are bi-directional, open drain signals, and are used to form a serial bus.

6 Output Protection

6.1 Over Current Protection: (OCP)

This power supply has current limit to prevent the outputs from exceeding the values shown in table below. If the current limits are exceeded the power supply will shut down and latch off. The latch will be cleared by toggling the PSON# signal or by an AC power interruption. This power supply will not be damaged from repeated power cycling in this condition. +5VSB will be auto-recovered after removing OCP limit.

| Output VOLTAGE | OVER CURRENT LIMITS | | |
|----------------|----------------------------|--|--|
| +3.3V | 110% minimum, 150% maximum | | |
| +5V | 110% minimum, 150% maximum | | |
| +12V | 110% minimum, 150% maximum | | |
| +5VSB | Minimum 4.5A | | |

6.2 Over Voltage Protection: (OVP)

This power supply over voltage protection will be locally sensed. This power supply will shut down and latch off after an over voltage condition occurs. This latch will be cleared by toggling the PSON# signal or by an AC power interruption. The values are measured at the output of the power supply's connectors. The voltage will never exceed the maximum levels when measured at the power connectors of the power supply connector during any single point of fail. The voltage will never trip any lower than the minimum levels when measured at the power connector. +5VSB will be auto-recovered after removing OVP limit.

| Output Voltage | MAX (V) |
|----------------|---------|
| +3.3V | 4.5 |
| +5V | 6.5 |
| +12V | 14.5 |
| -12V | -15 |
| +5VSB | 6.5 |

6.3 Over Temperature Protection: (OTP)

This power supply will be protected against over temperature conditions caused by loss of fan

cooling or excessive ambient temperature. In an OTP condition the PSU will shutdown. When the power supply temperature drops to within specified limits, this power supply will restore power automatically, while the +5VSB remains always on. The OTP circuit has built in margin such that the power supply will not oscillate on and off due to temperature recovering condition.

6.4 Short Circuit Protection: (SCP)

A short circuit placed on any DC output to DC return shall cause no damage. The power supply shall be latched in case any short circuit is taken place at +5V, +3.3V, +12V, -12Voutput. The power supply shall be auto-recovered in case any short circuit is taken place at +5VSB.

7 Environment

7.1 Temperature and Humidity

| Item | Description | MIN | MAX | Unit |
|----------------------|--|-----|-----|--------|
| T _{OP} | Operating temperature range | | 50 | °C |
| T _{non-OP} | Non-Operating temperature range | | 70 | °C |
| T_{Δ_change} | Rate of temperature change | | 20 | °C/hrs |
| H _{OP} | Operating humidity range, non condensing | 20 | 85 | % |
| H _{non-OP} | Non-Operating humidity range, non condensing | 10 | 95 | % |

7.2 Altitude

| Item | Description | MIN | ΜΑΧ | Unit |
|---------------------|------------------------------|-----|--------|------|
| A _{OP} | Operating Altitude range | 0 | 5,000 | m |
| A _{non-OP} | Non-Operating Altitude range | 0 | 15,200 | m |

7.3 Random Vibration

Non-operating

Sine sweep

5Hz to 500Hz @ 0.5gRMS at 0.5 octave/min; dwell 15 min at each of 3 resonant points;

Random profile

5Hz @ 0.01g²/Hz to 20Hz @ 0.02g²/Hz (slope up); 20Hz to 500Hz @ 0.02g²/Hz (flat);

Input acceleration = 3.13gRMS; 10 min. per axis for 3 axis on all samples

7.4 Mechanical Shock

Operating: 5G, no malfunction

Non-operating: 50G, no damage. Trapezoidal Wave, Velocity change = 4.3m/sec. Three drops in each of six directions are applied to each of the samples

8 Firmware Requirements

8.1 PMBus

8.1.1 Addressing

The PSU PMBus device address locations are shown below.

PSU PMBus Device Address Locations

| Addresses used: | | |
|--|----------------------|---------|
| System addressing A1/ A0 ³ | 0/0 | 0/1 |
| PMBus device read / write addresses ² | B0h/B1h ¹ | B2h/B3h |
| PSU PDB Device AAh/AB | | /ABh |

¹ Non-redundant power supplies will use the 0/0 address location

 2 The addressing method uses the 7 MSB bits to set the address and the LSB to define whether a device is reading or writing. The addresses defined above use 8 bits including the read/write bit.

³The '0' and '1' correspond to '1' = signal is not grounded; '0' = signal is grounded

8.1.2 PMBus Commands (Module)

The following PMBus commands shall be supported for the purpose of monitoring currents, voltages, and power. All sensors shall continue providing real time data as long as the PMBus device is powered. This means in standby mode the main output(s) of the power supply shall be zero amps and zero volts.

| Command | Command Name | SMBusb Transaction Type | Number Of Data | Data Format | Remark |
|---------|-----------------|-------------------------|----------------|-------------|---|
| Code | | | Bytes | | |
| 00h | PAGE | Read/Send Byte | 1 | | |
| 03h | CLEAR_FAULT | Send Byte | 0 | | |
| 05h | PAGE PLUS WRITE | Block Write | | | Used with STATUS_INPUT, STATUS_TEMPERATURE, |
| | | | | | STATUS_IOUT |
| | | Block Write-Block | | | Used with STATUS_INPUT, STATUS_TEMPERATURE, |
| 06h | PAGE_PLUS_READ | Read Process Call | | | STATUS_IOUT, STATUS_WORD |
| 19h | CAPABILITY | Read Byte | 1 | | |

| 1Ah QUERY Block Read 1 Image: Constraint of the second sec | <u>г </u> | | | | I | |
|---|--|--------------------|-------------------|----|-------------|--|
| Image: second | | | Block Write- | | | |
| Image: SMBALERT_MASK Write-Word_ABlock Image: SMBALERT_MASK Write-Biock Read Image: SMBALERT_MASK 1Bh SMBALERT_MASK Biock Read Image: SMBALERT_MASK Biock Read Image: SMBALERT_MASK 20h YOUT_MODE Read Byte 1 Image: SMBALERT_MASK Image: SMBALERT_MASK 20h YOUT_MODE Read Byte 1 Image: SMBALERT_MASK Image: SMBALERT_MASK 20h YOUT_MODE Read Byte 1 Image: SMBALERT_MASK Image: SMBALERT_MASK 30h COEFFICIENTS Block Read 5 Image: SMBALERT_MASK Image: SMBALERT_MASK 30h COEFFICIENTS Block Read 5 Image: SMBALERT_MASK Image: SMBALERT_MASK 30h COEFFICIENTS Block Read 1 Image: SMBALERT_MASK Image: SMBALERT_MASK 30h COEFFICIENTS Block Read 1 Image: SMBALERT_MASK Image: SMBALERT_MASK 30h COEFFICIENTS Block Read 1 Image: SMBALERT_MASK Image: SMBALERT_MASK 30h STATUS_IOUT Read/Write Byte 1 Image: SMBALERT_MASK Image: SMBALERT_MASK 7bh STATUS_OML Read/Write Byte 1 Image: SMBALERT_MASK Image: SMBALERT_MASK 7bh STATUS_OML <td>1Ah</td> <td>QUERY</td> <td>Block Read</td> <td>1</td> <td></td> <td></td> | 1Ah | QUERY | Block Read | 1 | | |
| 1Bh SMBALERT_MASK Write- 2 1Bh SMBALERT_MASK Block Read 2 20h VOUT_MODE Read Byte 1 20h VOUT_MODE Read Byte 1 30h COEFFICIENTS Block Read 5 30h COEFFICIENTS Block Read 5 33h FAN_CONFIG_1_2 Read Byte 1 38h FAN_CONFIG_1_2 Read Byte 1 38h FAN_COMMAND_1 ReadWrite Word 2 78h STATUS_BYTE Read Byte 1 78h STATUS_WORD Read Write Byte 1 79h STATUS_VOUT ReadWrite Byte 1 70h STATUS_COML ReadWrite Byte 1 70h STATUS_COML ReadWrite Byte 1 70h STATUS_OTHER ReadWrite Byte 1 70h STATUS_OTHER ReadWrite Byte 1 70h STATUS_COML ReadWrite Byte 1 70h STATUS_COML ReadWrite Byte 1 70h STATUS_COML ReadWrite Byte 1 70h READ_EIN Block Read 10 80h READ_EIN Block Read 10 </td <td></td> <td></td> <td>Process Call</td> <td></td> <td></td> <td></td> | | | Process Call | | | |
| 1Bh SMBALERT_MASK Block Read Block Read Process Call 20h VOUT_MODE Read Byte 30h COEFFICIENTS Block Write- 30h COEFFICIENTS Block Read 30h COEFFICIENTS Block Read 30h FAN_CONFIG_1_2 Read Byte 38h FAN_CONFIG_1_2 Read Write Word 38h FAN_COMMAND_1 Read Write Word 78h STATUS_BYTE Read Write Byte 78h STATUS_VOUT Read Write Byte 78h STATUS_OUT Read/Write Byte 78h STATUS_OUT Read/Write Byte 78h STATUS_OUT Read/Write Byte 78h STATUS_CML Read/Write Byte 78h STATUS_CML Read/Write Byte 78h STATUS_CML Read/Write Byte 78h STATUS_OTHER Read/Write Byte 78h STATUS_OTHER Read/Write Byte 78h STATUS_CML Read/Write Byte 78h STATUS_OTHER Read/Write Byte 78h STATUS_FAN_1_2 Read/Write Byte 78h STATUS_FAN_1_2 Read/Write Byte 81h STATUS_FAN_1_2 Read/Write Byte | | | Write Word /Block | | | |
| Biock Read Process Call 20h VOUT_MODE Read Byte 1 30h COEFFICIENTS Biock Read 5 30h COEFFICIENTS Biock Read 5 30h COEFFICIENTS Biock Read 5 33h FAN_CONFIG_1_2 Read Byte 1 38h FAN_COMMAND_1 ReadWord 2 78h STATUS_BYTE Read Word 2 78h STATUS_WORD ReadWord 2 78h STATUS_VOUT ReadWord 2 78h STATUS_VOUT ReadWite Byte 1 78h STATUS_OUT ReadWite Byte 1 78h STATUS_COUT ReadWite Byte 1 78h STATUS_COUT ReadWite Byte 1 78h STATUS_COLL ReadWite Byte 1 81h STATUS_FAN_1_2 ReadWite Byte 1 88h | 1Bb | SMBALERT MASK | Write- | 2 | | |
| 20h VOUT_MODE Read Byte 1 Image: Stratus and | | OMDALENT_MAON | Block Read | 2 | | |
| Block Write- Block Write- 30h COEFFICIENTS Block Read 5 3Ah FAN_CONFIG_1_2 Read Byte 1 3Bh FAN_CONFIG_1_2 Read Write Word 2 78h STATUS_BYTE Read Write Byte 1 79h STATUS_WORD Read/Write Byte 1 78h STATUS_VOUT Read/Write Byte 1 78h STATUS_VOUT Read/Write Byte 1 78h STATUS_OUT Read/Write Byte 1 78h STATUS_CML Read/Write Byte 1 89h READ_EN Block Read 10 88h READ_VIN Read/Word 2 Format 89h READ_JOUT Read/Word | | | Process Call | | | |
| 30h COEFFICIENTS Block Read 5 Image: Status S | 20h | VOUT_MODE | Read Byte | 1 | | |
| Image: second | | | Block Write- | | | |
| 3Ah FAN_CONFIG_1_2 Read Byte 1 1 3Bh FAN_COMMAND_1 Read/Write Word 2 1 78h STATUS_BYTE Read Word 2 1 79h STATUS_WORD Read/Write Byte 1 1 79h STATUS_VOUT Read/Write Byte 1 1 78h STATUS_LOUT Read/Write Byte 1 1 78h STATUS_IOUT Read/Write Byte 1 1 78h STATUS_CML Read/Write Byte 1 1 78h STATUS_OTHER Read/Write Byte 1 1 88h READ_EN Block Read 10 1 88h READ_EOUT Block Read 10 1 89h READ_INN Read Word 2 Format 88h READ_VOUT Read Word 2 Format 88h READ_VOUT Read Word 2 For | 30h | COEFFICIENTS | Block Read | 5 | | |
| 3Bh FAN_COMMAND_1 Read/Write Word 2 | | | Process Cal | | | |
| 78h STATUS_BYTE Read Byte 1 79h STATUS_WORD Read Word 2 7Ah STATUS_VOUT Read/Write Byte 1 7Bh STATUS_IOUT Read/Write Byte 1 7Bh STATUS_TEMPERATURE Read/Write Byte 1 7Dh STATUS_CML Read/Write Byte 1 7Fh STATUS_OTHER Read/Write Byte 1 7Fh STATUS_OTHER Read/Write Byte 1 81h STATUS_FAN_1_2 Read/Write Byte 1 86h READ_EIN Block Read 10 87h READ_EOUT Block Read 10 88h READ_VIN Read Word 2 89h READ_IN Read Word 2 89h READ_VOUT Read Word 2 88h READ_VOUT Read Word 2 88h READ_VOUT Read Word 2 88h READ_IOUT Read Word 2 88h </td <td>3Ah</td> <td>FAN_CONFIG_1_2</td> <td>Read Byte</td> <td>1</td> <td></td> <td></td> | 3Ah | FAN_CONFIG_1_2 | Read Byte | 1 | | |
| 79h STATUS_WORD Read Word 2 7Ah STATUS_VOUT Read/Write Byte 1 7Bh STATUS_IOUT Read/Write Byte 1 7Dh STATUS_TEMPERATURE Read/Write Byte 1 7Eh STATUS_OML Read/Write Byte 1 7Fh STATUS_OML Read/Write Byte 1 81h STATUS_FAN_12 Read/Write Byte 1 86h READ_EIN Block Read 10 88h READ_EOUT Block Read 10 89h READ_VIN Read Word 2 88h READ_UOUT Read Word 2 88h | 3Bh | FAN_COMMAND_1 | Read/Write Word | 2 | | |
| 7Ah STATUS_VOUT Read/Write Byte 1 Image: Status_IOUT 7Bh STATUS_IOUT Read/Write Byte 1 Image: Status_ICML 7Dh STATUS_CML Read/Write Byte 1 Image: Status_ICML 7Eh STATUS_OTHER Read/Write Byte 1 Image: Status_ICML 7Fh STATUS_OTHER Read/Write Byte 1 Image: Status_ICML 8th STATUS_FAN_1_2 Read/Write Byte 1 Image: Status_ICML 86h READ_EIN Block Read 10 Image: Status_ICML 87h READ_EOUT Block Read 10 Image: Status_ICML 88h READ_VIN Read Word 2 Linear Data 89h READ_IIN Read Word 2 Image: Status_ICML 88h READ_VOUT Read Word 2 Image: Status_ICML 88h READ_IOUT Read Word 2 Image: Status_ICML 88h READ_IOUT Read Word 2 Image: Status_ICML 88h READ_IOUT Read Word 2 Image: Status_ICML 88h READ | 78h | STATUS_BYTE | Read Byte | 1 | | |
| 7Bh STATUS_IOUT Read/Write Byte 1 Image: constraint of the syste 7Dh STATUS_TEMPERATURE Read/Write Byte 1 Image: constraint of the syste 7Eh STATUS_OTHER Read/Write Byte 1 Image: constraint of the syste 7Fh STATUS_OTHER Read/Write Byte 1 Image: constraint of the syste 8th STATUS_FAN_1_2 Read/Write Byte 1 Image: constraint of the syste 8th STATUS_FAN_1_2 Read/Write Byte 1 Image: constraint of the syste 8th STATUS_FAN_1_2 Read/Write Byte 1 Image: constraint of the syste 8th STATUS_EAN_1_2 Read/Write Byte 1 Image: constraint of the syste 8th READ_EOUT Block Read 10 Image: constraint of the syste 8th READ_VIN Read Word 2 Linear Data 8th READ_VOUT Read Word 2 Format 8th READ_LOUT Read Word 2 Format 8th READ_LOUT Read Word 2 Format 8th READ_TEMPERATURE_1 Read | 79h | STATUS_WORD | Read Word | 2 | | |
| 7Dh STATUS_TEMPERATURE Read/Write Byte 1 Image: Constraint of the state of the | 7Ah | STATUS_VOUT | Read/Write Byte | 1 | | |
| 7Eh STATUS_CML Read/Write Byte 1 Image: mathematical system of the system | 7Bh | STATUS_IOUT | Read/Write Byte | 1 | | |
| 7Fh STATUS_OTHER Read/Write Byte 1 Image: Constraint of the state | 7Dh | STATUS_TEMPERATURE | Read/Write Byte | 1 | | |
| 81h STATUS_FAN_1_2 Read/Write Byte 1 Image: Constraint of the system of the sys | 7Eh | STATUS_CML | Read/Write Byte | 1 | | |
| 86h READ_EIN Block Read 10 Image: Constraint of the state of the s | 7Fh | STATUS_OTHER | Read/Write Byte | 1 | | |
| $ \begin{array}{c c c c c c c c c c c c c c c c c c c $ | 81h | STATUS_FAN_1_2 | Read/Write Byte | 1 | | |
| 88h READ_VIN Read Word 2 Linear Data 89h READ_IIN Read Word 2 Format 89h READ_IIN Read Word 2 Linear Data 88h READ_VOUT Read Word 2 Format 88h READ_VOUT Read Word 2 Format 88h READ_VOUT Read Word 2 Format 88h READ_IOUT Read Word 2 Linear Data 88h READ_IOUT Read Word 2 Format 88h READ_IOUT Read Word 2 Format 88h READ_TEMPERATURE_1 Read Word 2 Format | 86h | READ_EIN | Block Read | 10 | | |
| 88h READ_VIN Read Word 2 89h READ_IIN Read Word 2 89h READ_IIN Read Word 2 88h READ_VOUT Read Word 2 88h READ_IOUT Read Word 2 80h READ_TEMPERATURE_1 Read Word 2 80h READ_TEMPERATURE_1 Read Word 2 | 87h | READ_EOUT | Block Read | 10 | | |
| Image: second | ooh | | Deed Word | 0 | Linear Data | |
| 89h READ_IIN Read Word 2 8Bh READ_VOUT Read Word 2 8Bh READ_VOUT Read Word 2 8Ch READ_IOUT Read Word 2 8Ch READ_IOUT Read Word 2 8Dh READ_TEMPERATURE_1 Read Word 2 8Dh READ_TEMPERATURE_1 Read Word 2 8Dh READ_TEMPERATURE_1 Read Word 2 | 0011 | READ_VIN | Read Word | 2 | Format | |
| Bh READ_VOUT Read Word 2 Linear Data 8Bh READ_VOUT Read Word 2 Format 8Ch READ_IOUT Read Word 2 Linear Data 8Ch READ_IOUT Read Word 2 Linear Data 8Dh READ_TEMPERATURE_1 Read Word 2 Format 8Dh READ_TEMPERATURE_1 Read Word 2 Format | ooh | | Deed Word | 0 | Linear Data | |
| 8Bh READ_VOUT Read Word 2 Image: Second state st | 890 | READ_IIN | Read word | 2 | Format | |
| BCh READ_IOUT Read Word 2 Linear Data 8Ch READ_IOUT Read Word 2 Format 8Dh READ_TEMPERATURE_1 Read Word 2 Linear Data 8Dh READ_TEMPERATURE_1 Read Word 2 Format | 05 | | | 2 | Linear Data | |
| 8Ch READ_IOUT Read Word 2 8Dh READ_TEMPERATURE_1 Read Word 2 Format Format | 8BN | READ_VOUT | Read Word | 2 | Format | |
| 8Dh READ_TEMPERATURE_1 Read Word 2 Linear Data Format | | | | 2 | Linear Data | |
| 8Dh READ_TEMPERATURE_1 Read Word 2 Image: Second se | 8Ch | KEAD_IOUT | Read Word | 2 | Format | |
| Format | | | | | Linear Data | |
| 8Eb READ TEMPERATURE 2 Road Word 2 Lincar Data | 8Dh | READ_TEMPERATURE_1 | Read Word | 2 | Format | |
| | 8Eh | READ_TEMPERATURE_2 | Read Word | 2 | Linear Data | |

| | | | | Format | |
|-------|--------------------|-------------|----------------|-------------|---------------------------|
| | | | | Linear Data | |
| 8Fh | READ_TEMPERATURE_3 | Read Word | 2 | | |
| | | | | Format | |
| 001 | | Deschalter | | Linear Data | |
| 90h | READ_FAN_SPEED_1 | Read Word | 2 | Format | |
| | | | | Linear Data | |
| 96h | READ_POUT | Read Word | 2 | | |
| | | | | Format | |
| | | | _ | Linear Data | |
| 97h | READ_PIN | Read Word | 2 | Format | |
| 0.01 | | | | | |
| 98h | PMBUS_REVISION | Read Byte | 1 | | |
| 99h | MFR_ID | Block Read | Variable(up to | ASCII | anky Block Dood for yours |
| 990 | | DIUCK Reau | 32 bytes) | ASCII | only Block Read for users |
| | | | Variable(up to | | |
| 9Ah | MFR_MODEL | Block Read | | ASCII | only Block Read for users |
| | | | 32 bytes) | | |
| | | | Variable(up to | | |
| 9Bh | MFR_REVISION | Block Read | 32 bytes) | ASCII | only Block Read for users |
| | | | | | |
| 9Ch | MFR_LOCATION | Block Read | Variable(up to | ASCII | only Block Read for users |
| | | Dictin toda | 32 bytes) | | |
| | | | Variable(up to | | |
| 9Dh | MFR_DATE | Block Read | | ASCII | only Block Read for users |
| | | | 32 bytes) | | |
| 9Eh | MFR_SERIAL | Block Read | Variable(up to | ASCII | anly Plack Dood for your |
| 9En | MFR_SERIAL | BIOCK Read | 32 bytes) | ASCII | only Block Read for users |
| | | | | Linear Data | |
| A0h | MFR_VIN_MIN | Read Word | 2 | | |
| | | | | Format | |
| | | | - | Linear Data | |
| A1h | MFR_VIN_MAX | Read Word | 2 | Format | |
| | | | | | |
| A2h | MFR_IIN_MAX | Read Word | 2 | Linear Data | |
| | | | | Format | |
| | | | | Linear Data | |
| A3h | MFR_PIN_MAX | Read Word | 2 | | |
| | | | | Format | |
| A4h | MFR_VOUT_MIN | Read Word | 2 | Linear Data | |
| 71411 | | | 2 | Format | |
| | | | | Linear Data | |
| A5h | MFR_VOUT_MAX | Read Word | 2 | | |
| | | | | Format | |

| A6h | MFR_IOUT_MAX | Read Word | 2 | Linear Data | |
|-----|--------------------------|---------------------|-----|-------------|--|
| | | | | Format | |
| A7h | MFR_POUT_MAX | Read Word | 2 | Linear Data | |
| | | | | Format | |
| A8h | MFR_TAMBIENT_MAX | Read Word | 2 | Linear Data | |
| | | | | Format | |
| A9h | MFR_TAMBIENT_MIN | Read Word | 2 | Linear Data | |
| | | | | Format | |
| ABh | MFR_EFFICIENCY_HL | Block Read | 14 | | |
| D0h | MFR_REDUNDANCY_SETTING | Read/Write Byte | 1 | | |
| DCh | MFR_BLACK_BOX | Block Read | 230 | | |
| DDh | MFR_REAL_TIME_BLACK_BOX | Block Write / Block | 4 | | |
| | | Read | | | |
| DEh | MFR_SYSTEM_BLACK_BOX | Block Write / Block | 40 | | |
| | | Read | | | |
| DFh | MFR_BLACK_BOX_CONFIG | Read/Write Byte | 1 | | |
| E0h | MFR_CLEAR_BLACK_BOX | Send Byte | 0 | | |
| FBh | MFR_PFC_FIRMWARE_VERSION | Read Word | 2 | Mfr | |
| FCh | MFR_SND_FIRMWARE_VERSION | Read Word | 2 | Mfr | |

Note: The PMBus commands can provide complete information under normal operation of the PSU. Some information may be distorted when the PSU is abnormal.

8.1.3 PMBus Commands (PDB)

| Command Code | Pages | Command Name | SMBus Transaction Type | Number Of Data Bytes |
|-----------------|---------|--------------------|------------------------|-------------------------|
| 00h | | PAGE | Read/Send Byte | |
| 8Bh | 00h~02h | READ_VOUT | Read Word | 2 |
| 8Ch | 00h~02h | READ_IOUT | Read Word | 2 |
| 8Dh | | READ_TEMPERATURE_1 | Read Word | 2 |
| 8Eh | | READ_TEMPERATURE_2 | Read Word | 2 |
| 96h | 00h~02h | READ_POUT | Read Word | 2 |

8.2 Page Define

00h: 12V output

01h: 5V output(PDB only)

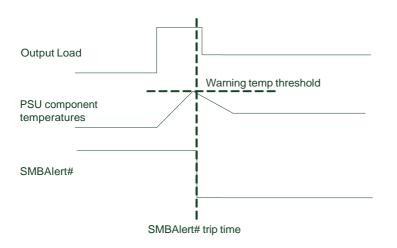
02h: 3.3V output(PDB only)

8.3 Sensors Accuracy(Module only)

| Sensor Functions | Accuracy | Accuracy | Accuracy |
|------------------|-------------|--------------|----------------|
| | 0-100% load | 40-200W load | 200W-Full load |
| READ_VIN | +/- 3% | | |
| READ_IIN | | | +/- 5% |
| READ_PIN | | +/- 10W | +/- 5% |
| READ_VOUT | +/- 3% | | |
| READ_IOUT | | +/- 1A | +/- 5% |
| READ_POUT | | +/- 10W | +/- 5% |
| READ_TEMPERATURE | +/- 3 °C | | |
| READ_FAN_SPEED | +/- 5 % | | |

8.4 Closed Loop System Throttling (CLST)

The power supply shall always assert the SMBAlert signal whenever any component in the power supply reaches a warning threshold. Upon reduction of the load within 2msec after the SMBAlert# signal is asserted if the load is reduced to less than the power supply rating; the power supply shall continue to operate and not shutdown.



8.5 Smart Ride-Through (SmaRT)

The power supply shall assert the SMBAlert signal < 2msec after AC input voltage is lost to 0VAC.

9 MTBF

The power supply shall have a minimum MTBF at continuous operation of 100,000 hours calculated at 100% load, according to MIL-HDBK-217F at 25°C excluding the Fan MTBF.

10 EMI

The power supply shall comply with FCC part 15, Subpart B and CE, EN55032+EN55024 Class A for both conducted and radiated emissions. Test shall be conducted using a shielded DC output cable to a shielded load. The load shall be adjusted to 100% load. Tests will be performed full load on each output power at 120VAC, 60Hz, and 230VAC, 50Hz.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.) Caution!

The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications to this equipment. Such modifications could void the user authority to operate the equipment.

11 Safety and EMC Compliance

- UL+cUL, UL 62368-1:2014
- TUV, EN62368-1:2014
- CB Certificate & Report, IEC60950-1 Edition 2, IEC62368-1:2014
- CCC(CQC China), GB4943-2011 Certification (China)

12 Mechanical

Physical dimension: 220mm (D) x 106mm (W) x 41.3mm (H)

13 Redundant Function

14.1 Hot Swap Requirements

Hot Swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages shall remain within the limits with the capacitive load specified. The hot swap test must be conducted when the system is operating

under static, dynamic and zero loading conditions. The power supply can be hot swapped by the following method:

Extraction: The power supply may be removed from the system while operating with PSON# asserted, while in standby mode with PSON# de-asserted or with no AC applied. No connector damage should occur during un-mating of the power supply from the power distribution board (PDB).

Insertion: The power supply may be inserted into the system with PSON# asserted, with PSON# de-asserted or with no AC power present for that supply. No connector damage should occur due to the mating of the output and input connector.

In general a failed (of by internal latch or external control) supply may be removed, then replaced with a good power supply, however, hot swap needs to work with operational as well as failed power supplies. The newly inserted power supply will get turned on into standby or Power On mode once inserted.

14.2 LED Indicators

The power supply uses a bi-color LED; Amber & Green. Below are table showing the LED states for power supply operating state.

| Power Supply Condition | LED State |
|---|-----------------|
| Output ON and OK | GREEN |
| No AC power to all power supplies | OFF |
| PSU standby state AC present / Only Standby on | 1Hz Blink GREEN |
| Power supply critical event causing a shutdown; failure, over current, short circuit, over voltage, fan failure, over temperature | AMBER |

14.3 TTL Indicators

There shall be an open-collect TTL to indicate power supply status. The TTL shall pull high to 5.0V indicate that all the power outputs are available or one module is dummy. The TTL shall pull low(under 1.0V) indicate that one module has failed or shutdown due to protection. The standard

backplane provides a single TTL outputs signal. There could have maximum 3 channels to external TTL output signal, TTL, TTL1 (reserved) and TTL2 (reserved).

| Channel name | | TTL | TTL1 | TTL2 |
|--------------|---|-------------|-----------------|-----------------|
| Status | | Total power | Module 1 status | Module 2 status |
| | | good status | (Left module) | (Right module) |
| | Support/Do not support | Support | Do not support | Do not support |
| Outpu | ut cable | TTL cable | Reserved | Reserved |
| | Action conditions | | | |
| NO. | Description | | | |
| 1 | Without anyone module input. | Low | Low | Low |
| 2 | Module 1 with AC or DC input, but without PS-ON, anyone module 2 without AC c DC input at housing. | Low | Low | Low |
| 3 | Module 2 with AC or DC input, but without PS-ON, anyone module 1 without AC c DC input at housing. | Low | Low | Low |
| 4 | Module 1 and 2 with AC or DC input at PS-ON on stage. | High | High | High |
| 5 | Module 1 with AC or DC input, and PS-ON, module 2 in the housing but without AC or DC input. | Low | High | Low |
| 6 | Module 2 with AC or DC input, and PS-ON, module 1 in the housing but without AC or DC input. | Low | Low | High |
| 7 | Module 1 with AC or DC input at PS-ON on stage, but without module 2. | Low | High | Low |
| 8 | Module 2 with AC or DC input at PS-ON on stage, but without module 1. | Low | Low | High |

| | Module 1 happen OVP, OCP, | | | |
|----|--------------------------------------|------|------|------|
| 9 | OTP, and Fan fail failure | Low | Low | High |
| | conditions, but modul ₆ 2 | Low | | |
| | working is normal. | | | |
| | Module 2 happen OVP, OCP, | | | |
| 10 | OTP, and Fan fail failure | Low/ | High | Low |
| | conditions, but modul ₆ 1 | Low | | |
| | working is normal. | | | |

14.4 Buzzer

The backplane has an audio buzzer to indicate that one module has failed or shutdown due to protection. The warning buzzer will sound continuously. It can reset warning buzzer by pressing the buzzer reset switch or by shorted (pull low) the buzzer reset connector.

| Power system condition | Backplane Buzzer | |
|---|------------------|--|
| No input AC or DC power to all PSU | OFF | |
| No input AC or DC power to one PSU only | Steady buzzing | |
| Input AC or DC present/only standby output on | OFF | |
| Power supply DC output ON and OK | OFF | |
| One power module failure or shutdown | Steady buzzing | |