IX-700RSH1UP8UC

Active PFC/Full Range Input

(1U 700W 1+1 Redundant)

SPECIFICATION

Revision: 1.0

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Revision History

Version	Date	Revision Description
0.1	**2017/10/07**	First Version
0.2	**2018/04/25**	Modify Module and PDB PMUS command code
0.3	**2018/11/23**	Add EEPROM FRU information
0.4	**2019/09/02**	Add 5VSB OCP, modified MTBF and peak load and delete EEPROM FRU.
0.5	**2019/09/23**	Update MTBF Condition and safety standard. Add TTL & Buzzer indicators.
0.6	**2019/10/03**	Update LED Indicators
0.7	**2019/12/17**	Update PMBus and Sensor Accuracy
0.8	**2019/12/19**	Delete Power Module specification description and move to Power Module specification
0.9	**2019/12/30**	PDB does not support over temperature protection function. Delete OTP function form PDB specification.
1.0	**2020/04/08**	Update Sensor Accuracy

1. General

This specification defines the performance characteristics and functions of a 700 watts 1U form factor of switch mode redundant power supply with Active PFC (Power Factor Correction) and PMBus (Power Management Bus). Support 1+1 operation.

- 80 PLUS Platinum Efficiency
- Active Power Factor PF≧0.95
- 0~50℃ Working Temperature
- Surge: 2KV(L/N-PE) & 1KV(L-N)
- Altitude : 5000M
- 1+1 Redundant Design
- PMBus™ Communication
- Protections: UVP、OVP、OCP、SCP
- MTBF >250,000 hours at 25℃ typical load
- Application: Server, Storage , Networking , IPC
- Meet IEC62368-1

Electrical Specification

MODEL			IX-700RSH1UP8UC				
AIRFLOW			Back To Front				
INPUT	Voltage Range		90~264Vac				
	Operation Voltage		100~240Vac				
	Frequency Range		47~63Hz				
	AC Current (Full Load)		8.0A/115Vac, 4A/230Vac at full load				
	Inrush Current		30A peak @115Vac, 50A peak @230Vac Cold start at full load				
	Power Factor(Typ.)		≥0.95/115Vac, ≥0.95/230Vac at full load				
	Leakage Current		<3.5mA/240Vac				
	Efficiency (Typ.)	20% Load	-				
		50% Load	-				
		100% Load	85%				
		Certification	-				
OUTPUT	DC Voltage		+12V	+5V	+3.3V	+5VSB	-12V
	Maximum Load		58.3A	20A	20A	3A	0.5A
	Minimum Load		1A	0A	0A	0.1A	0A
	Power Output		700W				
	Ripple & Noise		120mV	50mV	50mV	50mV	120mV

	Output Voltage Tolerance	**±5%**	**±5%**	**±5%**	**±5%**	**±5%**
	Line Regulation	**±1%**				
	Load Regulation	**±5%**				
	Turn On Time And Rise Time	**<3s,20ms@115Vac/230Vac at full load**				
	Hold Up Time	**≥12ms@115Vac at 70% load**				
PROTECTION	**Short Circuit Protection**	**Latch Off**				
	Over Current Protection	**Latch Off**				
	Over Voltage Protection	**Latch Off**				
ENVIRONMENT	**Operation Temperature**	**0 ~ 50˚C**				
	Storage Temperature	**-40 ~ 80˚C**				
	Humidity	**Operating: 20% ~ 90%RH non-condensing**				
		Non-Operating: 5% ~ 95%RH non-condensing				
	TEMP. Coefficient	**±0.03%/˚C (0~50˚C)**				
EMC	**FCC CFR Title 47 Part 15 Sub Part B EN55024/EN55032**	**Conducted Class B Radiated Class B**				
HI-POT	**Dielectric Withstand Voltage**	**3sec / 1.5KVAC or 2545VDC with a trigger limit of 10mA.**				
SURGE VOLTAGE	**EN61000-4-5**	**Line to Line : 1KV Line-to-Ground: 2KV, Performance Criteria B**				
OTHERS	**MTBF**	**250Khrs min SR332(25˚C)**				
	Dimension	**260mm (L) x 106mm (W) x 41.5mm (H)**				
	Weight	**2350g**				
	AC connector	**IEC320 C14 type 3pin connector**				
	DC output connector	**ATX**				

2. AC Input Requirement

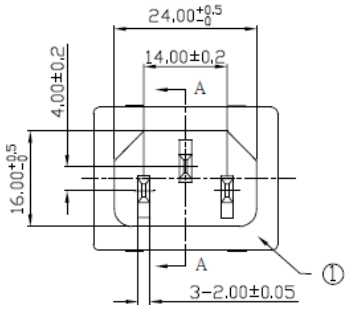
2.1 Input Voltage and Frequency

Voltage (sinusoidal): 100~240 VAC full range, with ±10% tolerance. Input frequency ranges from 47Hz~63Hz

2.2 Input AC Connector

The AC inlet is a IEC320 C14 type 3pin connector. This inlet shall be rated for operation at 10A/250VAC

Figure 1: AC Inlet



2.3 AC Input Current And Inrush Current

AC line inrush current shall not damage any component nor cause the AC line fuse to blow under any DC conditions and with any specified AC line input voltage and frequency. Inrush current is tested at 25 ℃ ambient and cold start within 1/4 AC cycle. Repetitive On/Off cycling of the AC input voltage shall not damage the power supply.

Table 1: Rated output power for each input voltage range

Parameter	Minimum Input	Input Voltage	Maximum Input	Brown In	Brown Out
115Vac	90Vac	100~120Vac	132Vac	85Vac ±5Vac	80Vac ±5Vac
230Vac	180Vac	200~240Vac	264Vac		
Frequency	47Hz	50/60Hz	63Hz		

Table 2: Maximum input current

Input Voltage	Input Current	Maximum Inrush Current	Max Power	Peak Power
90~132Vac	8.0A@115Vac	30A*peak@115Vac	700W	770W, ≤12ms
180~264Vac	4.0A@230Vac	50A*peak@230Vac	700W	770W, ≤12ms

*:Redundant Power Module

2.4 Input Power Factor Correction (Active PFC)

The power factor at 100% of rated load shall be ≥ 0.95 at nominal input voltage and full load.

2.5 AC Line Transient Specification

AC line transient conditions are characterized as “sag” and “surge” conditions. Sag conditions (also referred to as “brownout” conditions) will be defined as the AC line voltage dropping below nominal voltage. Surge conditions will be defined as the AC line voltage rising above nominal voltage. The power

supply shall meet the regulation requirements under the following AC line sag and surge conditions.

Table 3: AC Line Sag Transient Performance

Duration	Sag	Operating AC Voltage	Line Frequency	Load	Performance Criteria
Continuous	10%	115/230Vac	60/50 Hz	100%	No loss of function or performance
0 - ½ AC cycle	95%	115/230Vac	60/50 Hz	70%	No loss of function or performance
> 1 AC cycle	> 30%	115/230Vac	60/50 Hz	100%	Loss of function Acceptable, Self- recoverable

Table 4: AC Line Surge Transient Performance

Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	115/230Vac	60/50 Hz	No loss of function or performance
0 - ½ AC cycle	30%	115/230Vac	60/50 Hz	

3. DC Output Specification

3.1 Output Power / Currents

Table 5: Load Range

Voltage	Output Current			Condition
	Minimum Load	Maximum Load	Peak	
+12V	1A	58.3A	64A(≤12ms)	
+5V	0A	20A	22A(≤12ms)	The +3.3, +5 Volt total outputs shall not exceed 140W.
+3.3V	0A	20A	22A(≤12ms)	
+5VSB	0.1A	3A	N/A	
-12V	0A	0.5A	N/A	

* The +12V,+3.3V, +5V and -12Volt total outputs shall not exceed 700W.

3.2 Voltage Regulation, Ripple and Noise

Table 6: Regulation, Ripple and Noise

Output Voltage	+12V	+5V	+3.3V	+5VSB	-12V
Load Reg.	±5%	±5%	±5%	±5%	±5%
Line Reg.	±1%	±1%	±1%	±1%	±1%
Ripple & Noise	120mV	50mV	50mV	50mV	120mV

Ripple and noise shall be measured using the following methods:

- Measurements made differentially to eliminate common-mode noise
- Ground lead length of oscilloscope probe shall be ≤ 0.25 inch.
- Measurements made where the cable connectors attach to the load.
- Outputs bypassed at the point of measurement with a parallel combination of 10uF tantalum capacitor in parallel with 0.1uF ceramic capacitors at each point of measurement. The measurement points shall be as close as possible to the point of load..
- Oscilloscope bandwidth of 0 Hz to 20MHz.
- Measurements measured at locations where remote sense wires are connected.
- Regulation tolerance shall include temperature change, warm up drift and dynamic load

3.3 Capacitive Loading

The power supply shall operate within specifications over the capacitive loading ranges defined below in

Table 7: Capacitive Loading Conditions

Output	MIN	MAX	Units
+12V	10	11,000	uF
+5V	10	12,000	uF
+3.3V	10	12,000	uF
+5VSB	1	350	uF
-12V	1	350	uF

3.4 Dynamic Loading

The output voltages shall remain within the limits specified in Table-Regulation, ripple and noise for the step loading and within the limits specified in Table-Transient Load Requirement for the capacitive loading. The load transient repetition rate shall be tested between 50Hz and 5kHz at duty 50%. The load

transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load to the MAX load shown in Table-Load Range.

Table 8: Transient Load Requirements

Output	ΔStep Load Size	Load Slew Rate	Capacitive Load
+12V	50% of Max. Load	0.5 A/uS	2200 uF
+5V	30% of Max. Load	0.5 A/uS	1000 uF
+3.3V	30% of Max. Load	0.5 A/uS	1000 uF
+5VSB	50% of Max. Load	1.0 A/uS	1 uF

3.5 Overshoot at Turn-on/Turn-off

Any output overshoot at turn on shall be less than 10% of the nominal output value. Any overshoot shall recover to be within regulation requirements in less than 10ms.

3.6 Timing Requirements

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (Tvout_rise) within 1 to 20ms. For 5Vsb, it is allowed to rise from 1 to 25ms.Both outputs must rise monotonically. Refer to Figure 1 below which shows the timing requirements for the power supply being turned on and off via the input power, with PSON held low and the PSON signal, with the input power applied.

Figure 2: Turn On/Off Timing

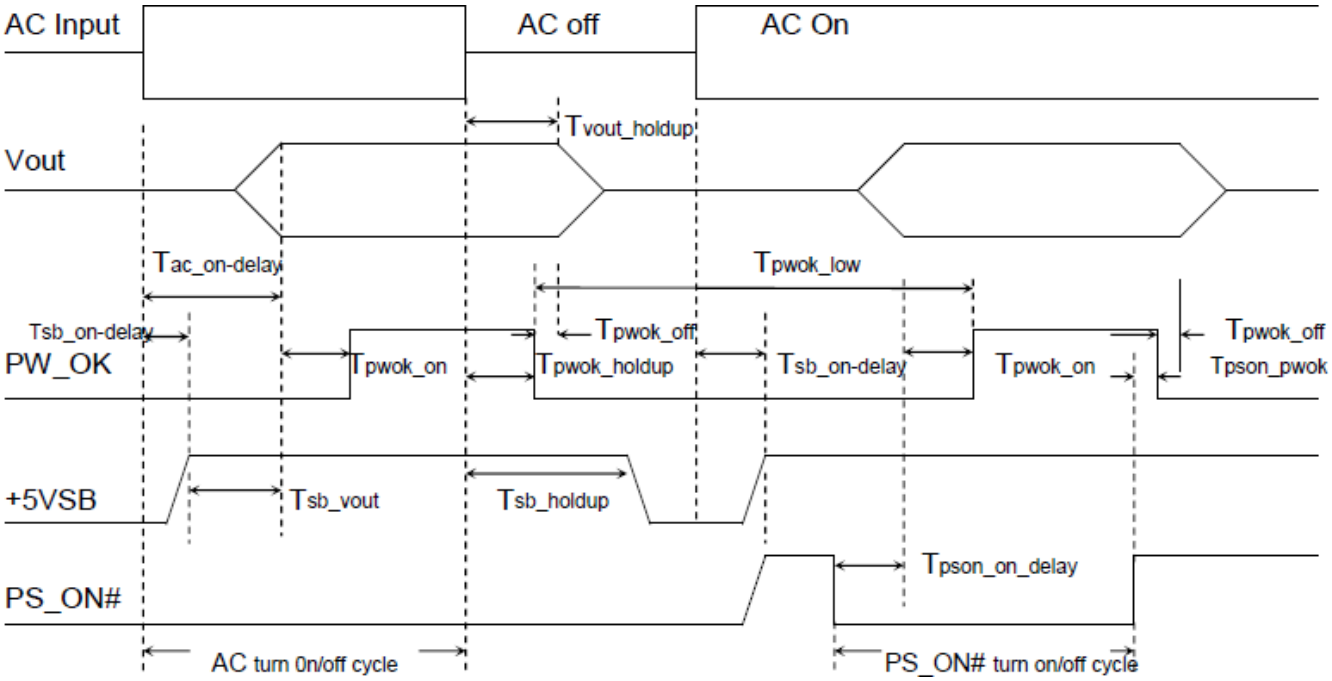


Table 9: Timing Requirements

Item	Description	MIN	MAX	UNITS
Tvout_rise	Output voltage rise time from each main output	1	20	mS
	Output voltage rise time for the 5Vsb out put	1	25	mS
Tsb_on-delay	Delay from AC being applied to +5Vsb being within regulation.		1500	mS
Tac_on-delay	Delay from AC being applied to all output voltages being within regulation.		2500	mS
Tvout_holdup	Time all output voltage stay within regulation after loss of AC tested at 70% load.	12		mS
Tpwok_holdup	Delay from loss of AC deassertion of PW_OK tested at 70% load.	11		mS
Tpson_on_delay	Delay from PS_ON# active to output voltage within regulation limits.	5	400	mS
Tpson_pwok	Delay from PS_ON# deactive to PW_OK being deasserted.		50	mS
Tpwok_on	Delay from output voltage within regulation limits to PW_OK asserted at turn on.	100	500	mS

Tpwok_off	Delay from PW_OK deasserted to output voltages dropping out of regulation limits tested at 70% load.	1		mS
Tpwok_low	Duration of PW_OK being in the deasserted state during an off/on cycle using AC or the PSON# signal. .	100		mS
Tsb_vout	Delay from +5Vsb being in regulation to O/Ps being in regulation at AC turn on.	50	1000	mS

3.7 Control Signal and Other DC Signals

3.7.1 PG Signal (PW_OK)

The power supply shall provide TTL compatible PW_OK signal to the system. Low pass filter (104 capacitor is recommended) shall be added into the PW_OK signal to suppress the high frequency noise to keep the high level absolutely. However, this low pass filter shall be used in PSU or motherboard PW_OK circuit. Therefore, supplier must be subject to add this low pass filter in the PW_OK input circuit of motherboard if it cannot be added in PSU circuit due to the re-layout difficulty.

Table 10: PW_OK TTL Characteristics

Signal Type	TTL Compatible Output Signal	
PW_OK = High	Power OK	
PW_OK = Low	Power Not OK	
	MIN	MAX
Logical low voltage , Isink = 20mA	0V	0.40V
Logical high voltage , Isource = 10mA	2.64V	3.46V
PW_OK rise and fall time	-	100uS

3.7.2 PS_ON# Signal

PS_ON# signal is required to remotely turn on/off the power supply module / PDB Combo. PS_ON# is an active low signal that turns on the +12V power rail and other DC to DC converters on the PDB. When this signal is not pulled low by the system, or left open, all the outputs (except for 5VSB) shall be turned off. This signal is pulled to a 3.3V voltage by a pull-up resistor internal to the PDB. Refer to Figure 11 On/Off Timing for timing diagram.

Table11: PS_ON# TTL Signal Characteristics

Note: When the ON / OFF switching of the PS_ON# signal, Interval cycle time must be > 1Sec.

Signal type	**Accepts an open collector/drain input from the system. Pull-up to VSB located in power supply.**	
PS_ON# = Low	Power ON	
PS_ON# = Open or High	Power OFF	
	MIN	MAX
Logic level low (power supply ON)	0V	0.8V
Logic level high (power supply OFF)	2.64V	3.46V
Source current, Vpson = low	-	4mA

Note: When the ON / OFF switching of the PS_ON# signal, Interval cycle time must be > 1Sec.

3.7.3 SMB_Alert# Signal

This signal indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events and that power supply is operating in an environment exceeding the specified limits. This signal is to be asserted in parallel with LED turning solid red.

Table12: SMB_ALERT# Signal Characteristics

Signal Type (Active Low)	**TTL Compatible Output Signal**	
SMB_Alert# = High	OK	
SMB_Alert# = Low	Alert to System	
	MIN	**MAX**
Logic level low voltage, Isink=4 mA	0V	0.4V
Logic level high voltage, Isource=50uA	2.64V	3.46V
Sink current, SMB_Alert# = low	-	4mA
Source current, SMB_Alert# = high	-	4mA
SMB_Alert# rise and fall time	-	100uS

3.7.4 SCL and SDA Signal

PMBus device uses System Management Bus (SMBus) Version 2.0, for transport layer, which is a two-wire communication protocol based on I2C. Both SCL and SDL lines are bi-directional, connected to

a positive supply voltage through a pull-up resistor or a current source.

Table13: SCL and SDA Signal Characteristics

Signal Type	TTL Compatible	
Operating Frequency	400KHz	
	MIN	**MAX**
Data Clock Input Low Voltage, (Vil)	0V	0.32V
Data Clock Input High Voltage (Vih)	2.64V	VDD
Data Clock Output Low Voltage (Vol)	-	0.4V
Input Leakage (Ileak)	-	±1uA
Current Through Pull-Up Resistor Or Current Source (Ipullup)	-	4mA
Nominal Bus Voltage (VDD)	-	3.46V

Note: For proper I2C communication, system designer must take account of all I2C devices connected to I2C bus and calculate appropriate pull-up resistors value that satisfy with above rating.

3.7.5 TTL Indicators

There shall be an open-collect TTL to indicate power supply status. The TTL shall pull high to 3.3V indicate that all the power outputs are available or one module is dummy. The TTL shall pull low(under 0.8V) indicate that one module has failed or shutdown due to protection. The standard backplane provides a single TTL output signal.

Power system condition	TTL Status
No AC input power to one power module	Low
One power module not inserted or pulled out	Low
AC Input present/only standby mode	Low
Power module PS ON and output normal	High
Any power module failure	Low

3.8 Efficiency

The power supply must be not less than 85% efficient at maximum load, tested at 230Vac/50Hz Input at 25 deg ambient condition.

FAN power is not included into total power consumption.

Efficiency is as follow :

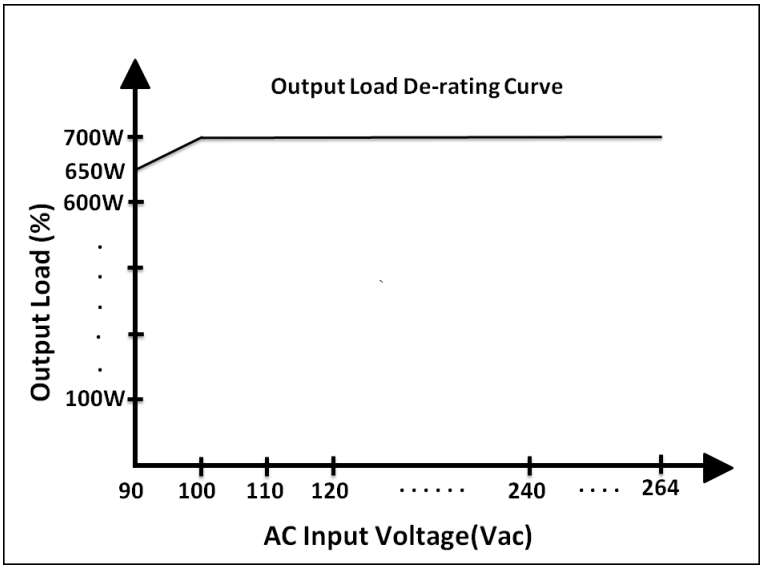
Table 14: Efficiency

Load	20% @230Vac	50% @230Vac	100% @230Vac
Efficiency (Module)	-	-	85%

3.9 Output Load De-rating Curve

When AC input operating under 100Vac,the power load need to following as below curve.

Figure 3



4. Protection Circuits

Protection circuits inside the power supply shall cause only the power supply's main outputs to shutdown. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15 sec and a PSON# cycle HIGH for 1 sec must be able to restart the power supply.

4.1 Over Current Protection (OCP)

The power supply shall have current limit to prevent the +12V outputs from exceeding the values shown in ***Table-Over Current Protection.*** The power supply shall latch off if the current exceeds the limit.

Table 15: Over Current Protection

Voltage	Minimum	Maximum	Shutdown Mode
5VSB (1+1)	3.2A	9A	Auto-recovery
+12V , +5V , +3.3V	110%	130%	Latch Off

4.2 Over Voltage Protection (OVP)

The power supply is protected against over voltage due to an internal regulator failure. When an over voltage condition is detected, all DC outputs are disabled (except the +5 Vsb). The fault must be removed to restore the DC outputs. The Limits set forth in the following table.

Table 16: Over Voltage Protection

Voltage	Minimum	Maximum	Shutdown Mode
+12V	+13.3V	+14.5V	Latch Off
+5V	+5.5V	+6V	Latch Off
+3.3V	+3.9V	+4.5V	Latch Off

4.3 Short Circuit Protection

- The power supply shall be no physical damage when +12V, +3.3V and +5V, is shorted to its DC return.
- +5Vsb shall be Auto Restart when short condition is removed.

4.4 No Load Operation

No damage or hazardous condition should occur with all the DC output connectors disconnected from the load.

5. Environmental Requirements

5.1 Temperature

Operating Ambient, normal mode (inlet air): 0°C ~ 50°C (32°F~ 131°F)

Non-operating Ambient:: -40°C ~ 80°C (-40°F~ 176°F)

5.2 Humidity

Operating: 20% ~ 90%RH non-condensing

Non-Operating: 5% ~ 95%RH non-condensing

5.3 Altitude

Operating: 16,404 ft (5000M)

5.4 Mechanical Shock

Non-Operating: 50 G Trapezoidal Wave, 11mS half sin wave. The shock is to be applied in each of the orthogonal axes.

5.5 Vibration (Non-Operating)

The power supply shall be subjected to a vibration test consisting of a 10 to 300 Hz sweep at a constant acceleration of 2.0g for duration of one (1) hour for each of the perpendicular axes X, Y and Z (0.1 octave/minute). The output voltages shall remain within specification.

5.6 Reliability

The MTBF of the power supply shall be calculated utilizing the Part-Stress Analysis method of SR332. The calculated MTBF of the power supply shall be greater than 250,000 hours under the following Conditions: Full rated load; 120V AC input; Ground Benign; 25°C; Without Fan

5.7 Electromagnetic Compatibility

Table 17: EMC Requirements

Electromagnetic Interference	FCC CFR Title 47 Part 15 Sub Part B EN55032/EN55024	Conducted Class B Radiated Class B		
Harmonics	IEC61000-3-2 Class D			
Flicker	IEC61000-3-3			
ESD Susceptibility	EN-61000-4-2	±8KV by Air, ±4KV by Contact Performance Criteria B		
Radiated Susceptibility	EN61000-4-3	80MHz~1000MHz (3V/m(mns) Amplitude 80% AM 1KHz Criteria A		
EFT/Burst	EN61000-4-4	5KHz, AC: 1KV, DC: 0,5 KV, Performance Criteria B		
Surge Voltage	EN61000-4-5	Line to Line : 1KV Line-to-Ground: 2KV, Performance Criteria B		
Conducted Susceptibility	EN61000-4-6	0.15MHz~80MHz 3V/m Amplitude 80% AM 1KHz Performance Criteria A		
RF Conducted	EN61000-4-8	50 Hz/3A(ms)/m Performance Criteria A		
Voltage Dips and Interruptions	EN61000-4-11	30%(Voltage Dips) 60%(Voltage Dips) >95%(Voltage Dips)	10 ms 100ms 500ms	Criteria B Criteria C Criteria C
Leakage Current	EN60950-1	3.5mA@240VAC		

5.8 Safety Agency Requirements

This power supply is designed to meet the following safety

Table 18: Product Safety

Product Safety:	• CB: IEC 60950-1:2005 (2nd Edition); Am 2:2013 • TUV: EN60950-1/A12:2011 • UL: UL60950-1, 2nd Edition, 2011-12-19; • UL62368-1, 2nd Edition, 2014-12-01 • IEC62368-1

6.PMBus Command Codes

6.1 PMBus Command Codes For Module

(Detailed settings, please refer to the Module Description)

6.2 PMBus PDB Address Table

Table 19 - PMBUS address Set Table (PDB)

PSU Model Name	Address
PSU PDB Device	BEh

Note: 1. Address Set “0” = Pin Connects to GND
2. Address Set “1” = Pin through resistor pulled up to 3.3V (Typical resistance range: 1K ~ 4K7)

6.3 PMBus Command Codes Table For PDB

Table 20 – PMBus Command Codes (PDB)

Command Code	Command Name	SMBus Transaction Type	Number of Data Bytes	Decode Format
19h	CAPABILITY	Read Byte	1	Byte
20h	VOUT_MODE	Read Byte	1	Byte
79h	STATUS_WORD	Read Word	2	Word
7Ah	STATUS_12V_VOUT	Read Byte	1	Byte
7Bh	STATUS_12V_IOUT	Read Byte	1	Byte
80h	STATUS_MFR_SPECIFIC	Read Byte	1	Byte
8Bh	READ_12V_VOUT	Read Word	2	Linear Vout
8Ch	READ_12V_IOUT	Read Word	2	Linear
8Dh	READ_TEMPERATURE_1 (1)	Read Word	2	Linear
96h	READ_12V_POUT	Read Word	2	Linear
99h	MFR_ID	Block Read	6	ASCII
9Ah	MFR_MODEL	Block Read	9	ASCII
9Bh	MFR_REVSION	Block Read	2	ASCII
9Eh	MFR_SERIAL	Block Read	12	ASCII
A7h	MFR_POUT_MAX	Read Word	2	Linear
A8h	MFR_AMBIENT_MAX	Read Word	2	Linear
B0h	STATUS_PDB	Read Byte	1	Byte
E0h	READ_3V3_VOUT	Read Word	2	Linear Vout
E1h	READ_3V3_IOUT	Read Word	2	Linear
E2h	READ_3V3_POUT	Read Word	2	Linear
E3h	READ_5V_VOUT	Read Word	2	Linear Vout
E4h	READ_5V_IOUT	Read Word	2	Linear
E5h	READ_5V_POUT	Read Word	2	Linear

Note : 1.Here READ_TEMPERATURE_1 is from PDB’s temperature.

Table 21 - Contents in 7Ah (STATUS_VOUT) Command Code

Bit Number	Status Bit Name	Meaning
7	VOUT_OV_FAULT(12V)	VOUT > 14V = 1 ; Normal = 0
6	VOUT_OV_WARNING(12V)	VOUT > 13.2V = 1 ; Normal = 0
5	VOUT_UV_WARNING(12V)	VOUT < 10.8 V = 1 ; Normal = 0
4	VOUT_UV_FAULT(12V)	VOUT < 8.4 V = 1 ; Normal = 0
[3:0]	Reserved	Return=0

Table 22 - Contents in 7Bh (STATUS_IOUT) Command Code

Bit Number	Status Bit Name	Meaning
7	IOUT_OC_FAULT(12V)	12V_IOUT > 70A of 110~ 150% = 1 ; Normal = 0
6	Reserved	Return=0
5	IOUT_OC_WARNING(12V)	12V_IOUT > 64A of 110% = 1 ; Normal = 0
[4:1]	Reserved	Return=0
0	Reserved	Return=0

Table 23: Contents in 80h (STATUS_MFR_SPECIFIC)Command Code

Bit Number	*Status Bit Name*	*Meaning*
7	3V3_UV_FAULT	VOUT < 2.8V = 1 ; Normal = 0
6	3V3_OV_FAULT	VOUT > 4.5V = 1 ; Normal = 0
5	5V_UV_FAULT	VOUT < 3.5V = 1 ; Normal = 0
4	5V_OV_FAULT	VOUT > 6.5V = 1 ; Normal = 0
3	3V3_IOUT_OC_ FAULT	3V3_IOUT > 24A = 1 ; Normal = 0
2	3V3_IOUT_OC_ WARNING	3V3_IOUT > 22A = 1 ; Normal = 0
1	5V_IOUT_OC_ FAULT	5V_IOUT > 24A = 1 ; Normal = 0
0	5V_IOUT_OC_ WARNING	5V_IOUT > 22A = 1 ; Normal = 0

Table 24: Contents in B0h (STATUS_PDB)Command Code

Bit Number	Status Bit Name	Meaning
7	PSU1_FAULT	PSU1 FAULT = 1 ; Normal = 0
6	PSU2_FAULT	PSU2 FAULT= 1 ; Normal = 0
5	PSU1 PLUG-IN/OUT_STATUS	PSU1 PLUG-OUT= 1 ; PLUG-IN = 0
4	PSU2 PLUG-IN/OUT _STATUS	PSU2 PLUG-OUT= 1 ; PLUG-IN = 0
3	POWER_GOOD#	POWER_GOOD signal is FAIL= 1; OK = 0
2	PSON#	PSON#_H = 1 ; PSON#_L = 0;
[1:0]	Reserved	Return=0

Table 25: Contents from 99h to A8h command code. MFR Information (PDB)

Command Code	Command Name	Meaning	Number of Data Bytes	Data Format
A7h	MFR_POUT_MAX	700 (W)	2	Linear
A8h	MFR_AMBIENT_MAX	50 (°C)	2	Linear

6.4 Sensor Accuracy

The sensor of the power supply shall meet below accuracy requirements for sensor readings.

Accuracy			
Item	0-100% load	40-200W load	200W-Full load
Vin	±5%		
Iin			±8%
Pin		±10W	±5%
Vout	±5%		
Iout		±1A	±5%
Pout		±10W	±5%
Temp.	±5℃		

7. MFR Information

The PMBus protocol provides commands for the storage and retrieval of the device manufacturer's inventory information. This is more typically the manufacturer of an assembled power supply or dc-dc converter than an IC manufacturer. The length of data for type of inventory information varies from manufacturer to manufacturer so the length of the data for each type is not specified. Instead, if a PMBus device supports manufacturer's inventory information, the device's product literature will state the total space available, in bytes, for all inventory information.

For PDB MFR information, please refer to table 25 respectively.

8. LED Indicators

There will be a LED on each power module to indicate power status

(Detailed settings, please refer to the Module Description)

9. Buzzer Indicators

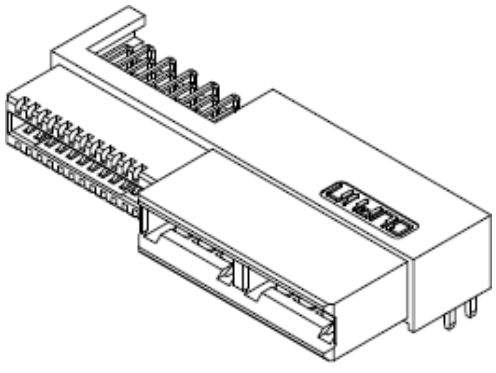
The backplane has an audio buzzer to indicate that one module has failed or shutdown due to protection. The warning buzzer will sound continuously. It can reset warning buzzer by pressing the buzzer reset switch or by shorted (pull low) the buzzer reset connector.

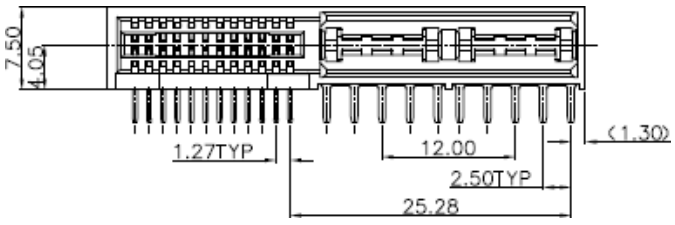
Power system condition	Backplane Buzzer Status
No AC input power to one power module only after PS ON	Steady buzzing
One power module not inserted or pulled out	Steady buzzing
AC Input present/only standby mode	OFF
Power module PS ON and output normal	OFF
Any power module failure after PS ON	Steady buzzing

10. PDB Mating Connector

The power supply shall have a card edge to mate with the Low Profile Hybrid Power connector Interconnect system. The Matting connector at PDB side is Oupiin 9392-4S24P04N12CB30DA or Molex 45984 Series

Figure 4: DC Connector





10.1 Pin Assignment of DC Connector (Bottom Side)

Figure 5 – Card Edge Pin Out Location

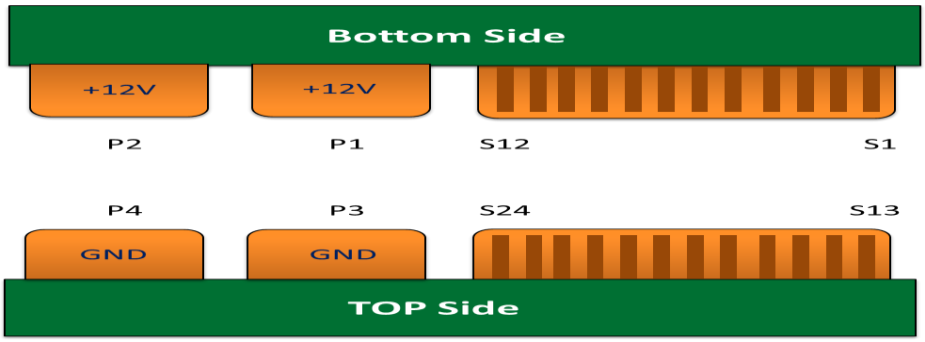


Table 26– Card Edge Pin Out Definition

Bottom Side			
Pin Name	**Signal Name**	**Function**	**System/Backplane Connection**
P1	+12V	+12V power output	TO SYSTEM 12V BUS
P2	+12V	+12V power output	TO SYSTEM 12V BUS
S1	12VRS+	+12V Remote sense	TO SYSTEM 12V BUS
S2	Reserved	Reserved	
S3	12VSHR	12V Load Share	Connect pin to pin at backplane for each power module
S4	SMB_ALERT#	If PSU FAIL,FAN FAIL,OCP occurs, signal will be pulled from High to Low , PSU normal =High(TTL LEVEL)	To system related bus
S5	SDA	I2C DATA	TO SYSTEM I2C BUS
S6	SCL	I2C CLOCK	TO SYSTEM I2C BUS
S7	PS_KILL	Activate PSU by hot-plug activity	Grounded at backplane
S8	PS_ON#	Module PS_ON#. Remote control power On/Off (Pulled LOW = POWER ON)	From System On/Off Controller
S9	PWR_OK	Power Good Output. Signal is pulled HIGH to indicate all outputs ok.	TO SYSTEM Power Good
S10	A1	I2C Address	
S11	+5VSB	+5V standby power	TO SYSTEM 5VSB BUS
S12	+5VSB	+5V standby power	TO SYSTEM 5VSB BUS

10.2 Pin Assignment of DC Connector (TOP Side)

Figure 6– Card Edge Pin Out Location

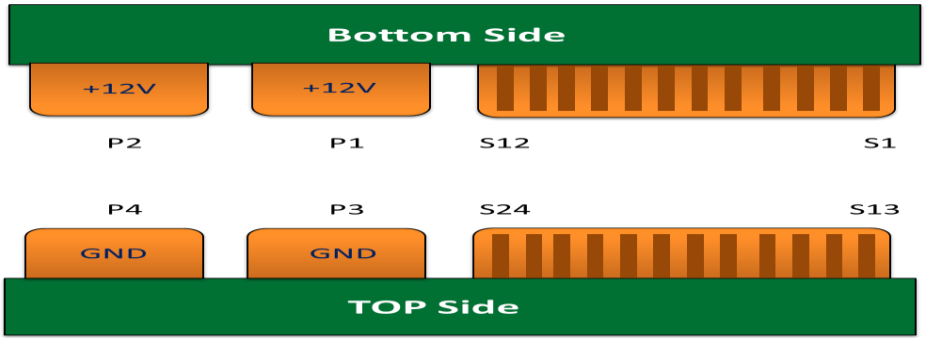


Table 27 – Card Edge Pin Out Definition

TOP Side			
Pin Name	**Signal Name**	**Function**	**System/Backplane Connection**
P3	GND	Grounding	GND
P4	GND	Grounding	GND
S13	Reserved	Reserved	
S14	PRESENT	This pin is grounded. To indicate a power has been plugged in.	Floating via backplane.
S15	A0	I2C Address	
S16	Reserved	Reserved	
S17	Reserved	Reserved	
S18	Reserved	Reserved	
S19	Reserved	Reserved	
S20	Reserved	Reserved	
S21	Reserved	Reserved	
S22	Reserved	Reserved	
S23	+5VSB	+5V standby power	TO SYSTEM 5VSB BUS
S24	+5VSB	+5V standby power	TO SYSTEM 5VSB BUS

Appendix I. Data Format Description

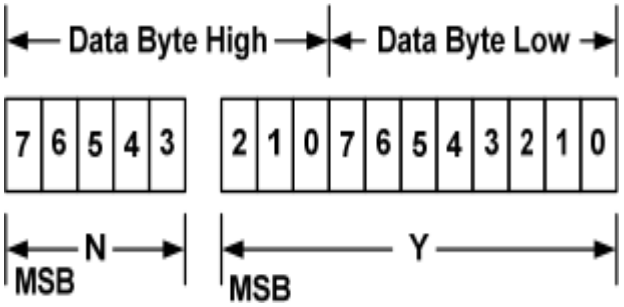
The Linear Data Format is typically used for commanding and reporting the parameters such as (but not only) the following:

- Input Voltage (V)
- Input Current (A)
- Input Power (W)
- Output Current (A)
- Output Power(W)
- FAN Speed (RPM)
- Temperature(℃)
- Any Warning Limit

The Linear Data Format is a two byte value with:

An 11 bit, two's complement mantissa and a 5 bit, two's complement exponent (scaling factor).

The format of the two data bytes is illustrated in Figure



The relation between Y, N and the "real world" value is:

$X = Y \cdot 2^N$

Where, as described above:

X is the "real world" value;

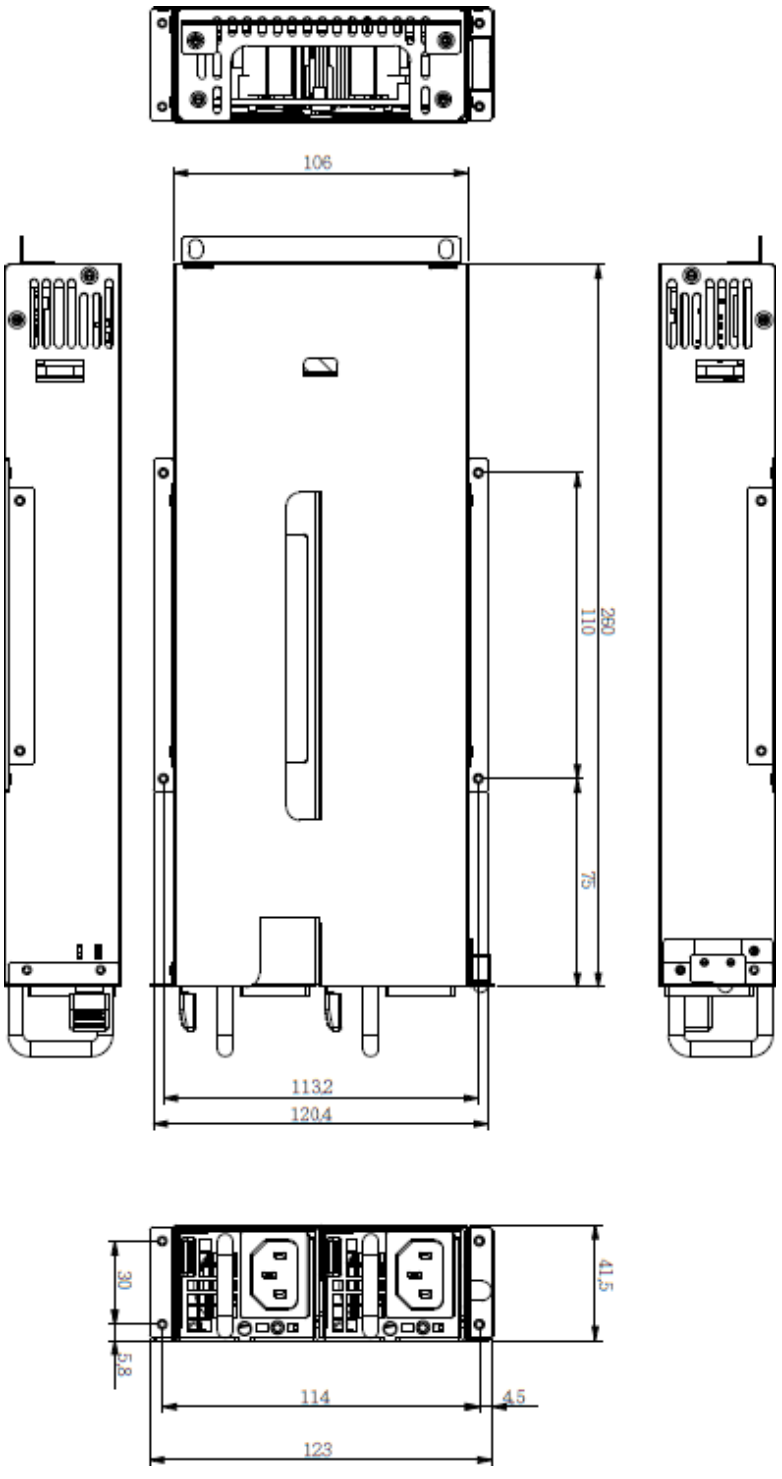
Y is an 11 bit, two's complement integer; and

N is a 5 bit, two's complement integer.

Devices that use the Linear format must accept and be able to process any value of N.

11. Mechanical Drawing

Size: 260mm (L) x 106mm (W) x 41.5mm (H)


106
260
110
75
113.2
120.4
30
5.8
114
4.5
123
41.5